Diamond & Related Materials xxx (2009) xxx–xxx

Contents lists available at ScienceDirect

Diamond & Related Materials

journal homepage: www.elsevier.com/locate/diamond

Formation and characterization of 4-inch GaN-on-diamond substrates

D. Francis [a], F. Faili [a], D. Babić [a,*], F. Ejeckam [a], A Nurmikko [b], H. Maris [b]

[a] Group4 Labs, Inc. 1600 Adams Dr., Menlo Park, CA, United States
[b] Dept. of Physics, Brown University, 184 Hope Street, Providence, RI, United States

ARTICLE INFO

Available online xxxx

Keywords:
Gallium nitride
CVD diamond
Wafer bow
Gan-on-diamond wafers

ABSTRACT

This paper reports on the first demonstration of four-inch gallium nitride (GaN) on 100-micron CVD diamond substrates and the characterization of the interface between the GaN and the diamond. Currently, gallium nitride devices are used for microwave power amplification at frequencies of up to 100 GHz. The very high thermal conductivity of diamond enables the increase in power and improvement in lifetime and reliability of the amplifiers by efficiently removing the heat from the active region of devices fabricated on GaN-on-diamond substrates. While we have previously demonstrated and currently are producing 2-inch GaN-on-diamond wafers. Increasing the diameter of GaN-on-diamond substrate is both non-trivial and essential for entry into high-volume GaN electronics manufacturing. Since the primary significance of the GaN-on-diamond structure lies in its ability to efficiently remove the heat from the active regions, the state and quality of the bond between the GaN, the diamond, and any enabling adhesion layers are critical in the transmission of heat through the interface and the reliability of the completed devices. In this paper, in addition to the discussion of challenges associated with the scale-up, we characterize the interfacial bonding between the critical layers using a picosecond ultrasonic measurement technique. The measurements indicate excellent adhesion of the interlayer to both the GaN and to the diamond. The qualified substrates from this exercise were used in fabrication of devices that have demonstrated transition frequencies of up to 85 GHz. These findings should help to further the development of GaN-on-diamond technology on the path to commercialization for high-power, high-frequency amplifiers.

© 2009 Elsevier B.V. All rights reserved.

1. Introduction

The commercialization of gallium-nitride (GaN) technology in recent decades has opened doors for the realization of a variety of new optoelectronic and electronic devices [1–4]. While high-efficiency optoelectronic devices, such as, light-emitting diodes and lasers, operating in blue and ultraviolet wavelength range are already in production, high-power field-effect transistors for RF and millimeter-wave applications for wireless communications and radar are just now entering the market. GaN properties make it an inherently superior material to silicon and gallium arsenide for high-power electronic applications. However, the full realization of superior properties of GaN is limited by the thermal conductivity of the substrates on which GaN is grown. Commercial substrates for GaN epilayers include sapphire, silicon, and silicon carbide. These commercial substrates have thermal conductivities between 40 and 400 W/mK. With thermal conductivity values ranging from 800 to 1800 W/mK, chemical vapor deposited (CVD) diamond provides GaN with a substrate that has far superior heat spreading properties compared to that of single-crystal silicon carbide or any other commercially available substrate. Consequently, engineered wafers in which GaN epilayers are atomically attached to CVD diamond substrates, referred to as GaN-on-diamond wafers, offer potentially optimal heat spreading for GaN devices. Using GaN-on-diamond wafers, electronic systems can expect an increase in power handling capacity that would significantly reduce system-level cooling costs and packaging challenges. For this reason, in recent years we have seen a substantial surge in attempts at variety of approaches that target the integration of these two materials [5–11].

Having previously demonstrated the technology for fabrication of 2-inch GaN-on-diamond wafers [5], we report on the first successful demonstration of a 4-inch GaN-on-100 micron-thick diamond wafers. In this article, Section 1 discusses the choice of diamond thickness, Section 2 discusses the managing of the wafer bow and warp resulting from the difference in thermal expansion of the materials involved, and Section 3 discusses the results of the characterization of the GaN and CVD diamond interface using the picosecond acoustic phonon measurement technique.

2. Analysis of the effect of diamond thickness as a function of chip size

The typical use of diamond heat-spreaders in the electronics industry involves soldering the die to a heat spreader and attachment of the heat spreader to a heat-sink. Optimal heat-spreading from dies with sizes ranging from several hundred micrometers to several

* Corresponding author.
E-mail address: dubravko.babic@group4labs.com (D. Babić).

0925-9635/$ – see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.diamond.2009.08.017

ARTICLE IN PRESS

millimeters requires diamond heat-spreaders with dimensions that are comparable to the die size [12] and thickness in excess of 500 µm. These dimensional requirements make conventional diamond heat-spreaders very costly, while the need for polishing of such heat spreaders adds to the final cost [13]. Additionally, the thickness of the solder layer results in an increase in thermal resistance that directly impacts the performance of the device. GaN-on-diamond technology offers a different approach: by virtue of the GaN and diamond bonding to within nanometers, the chip itself is a heat-spreader with a heat source which is much smaller than the chip, allowing for the use of a dramatically thinner and dimensionally smaller chip/heat spreaders. This technology has two distinct advantages: (1) a more efficient thermal management due to the proximity of the heat spreader to the heat source; and (2) a lower price per chip since both the diamond and the chip are smaller.

The typical structure of a GaN HEMT includes multiple gate fingers of length that varies between 50 µm and 150 µm. Devices operating at lower frequencies (C-band, wireless) tend to have longer gate-finger widths, while millimeter-wave devices are designed with smaller gate-finger widths to reduce the phase lag. Devices with multiple fingers employ a linear array of gate-fingers perpendicular to the direction of each finger. The gate finger width and the die size have a profound effect on the efficiency of heat spreading. To estimate the optimum diamond thickness for heat extraction, we selected to model a typical gate-finger (125 µm wide and 2 µm long) and estimated the heat spreading of a single finger (single-line heat source) on a diamond heat spreader attached to a copper heat-sink on a constant temperature background. The modeled structure is shown in Fig. 1. In our analysis, we varied the thickness and the total width of the diamond heat-spreader. This simple model allowed us to estimate the optimal thickness of the diamond layer for a typical gate-finger width. It should be noted that introducing multiple fingers to this structure, i.e., forming an array of heat sources, widens the heat source only in one direction, making the chip width grow with the total width of the transistor. Therefore, as long as the total lateral separation of the gates does not exceed the width of the transistor, the results of single-finger estimated heat spreader thickness stays valid for the multi-finger structures.

In our analysis, we varied the total width of the chip as well as the diamond thickness to observe the thermal resistance variation as a function of these two variables. We approximated the chip as a cylinder to maintain simplicity in the calculations and presentation. The results are shown in Fig. 2. If the chip diameter (or its lateral size) were infinite adding more diamond thickness would monotonically decrease the thermal resistance as more volume would become available for heat spreading even though the improvement may be infinitesimal. If we limit the size of the chip, the spreading resistance will saturate while the thermal resistance of the laterally constricted cylinder will grow with the thickness, this is primarily due to the finite thermal conductivity of the diamond. The thermal resistance of the constricted cylinder is commonly referred to as the 1D conduction heat resistance [13].

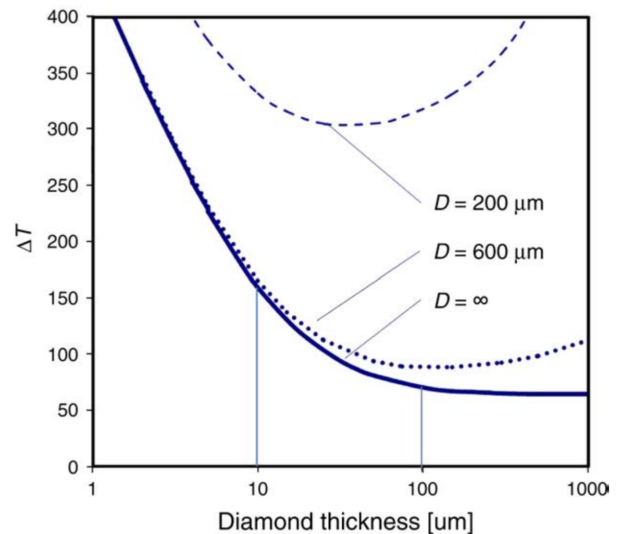

Fig. 2. Modeling results showing the transistor peak temperature as a function of the diamond thickness for various chip sizes.

The most significant result observed in Fig. 2 is that the heat-spreading contribution has largely saturated when the diamond thickness is approximately equal to the characteristic dimension of the heat source — in this case the length of the gate finger, or approximately 100 µm. These estimates are consistent with detailed numerical calculations observed by other researchers [12]. Based on this analysis, we conclude that 100 µm is a good choice for the thickness of a diamond substrate for a typical GaN HEMT. Fig. 2 also demonstrates that a chip width of 600 µm is sufficient to provide major heat-spreading benefits of the diamond, while a smaller chip width could severely constrict effective heat spreading.

Though approximate, the calculation presented here strongly suggests, that to achieve the lowest possible thermal resistance in GaN-on-diamond structures, both the chip size and its lateral dimensions has to be optimized.

3. Discussion of the formation of GaN-on-diamond wafers and the effects of thermal expansion

3.1. Building GaN-on-diamond

Formation of GaN-on-diamond wafers was previously described in reference [5] and is schematically illustrated in Fig. 3. To build the wafer, we start with GaN HEMT epitaxial layers (typically 2 µm

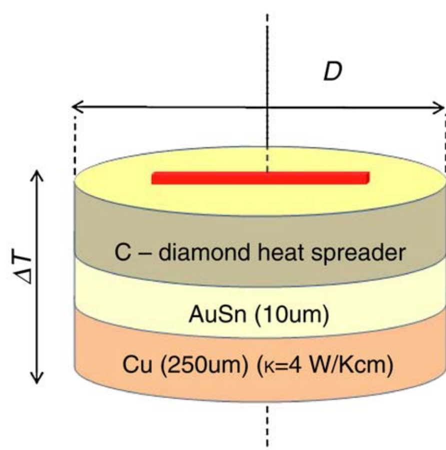

Fig. 1. Schematic of the modeled structure.

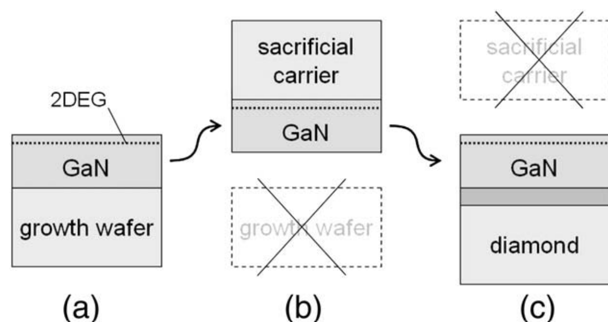

Fig. 3. GaN-on-diamond process illustration.

Please cite this article as: D. Francis, et al., Diam. Relat. Mater. (2009), doi:10.1016/j.diamond.2009.08.017

ARTICLE IN PRESS

thick) grown on silicon, as shown in step (a) of Fig. 3. In order to preserve the orientation of the epilayers, which is required to fabricate HEMTs on this structure, we perform an epilayer transfer twice. We refer to this as the *double-flip* process. In the *double-flip* process, we bond the GaN-epilayer structure in step (a) to another silicon wafer forming a silicon-GaN-silicon wafer stack. The second silicon wafer serves as a sacrificial carrier for the GaN epilayers and allows us to remove the growth silicon substrate. The growth silicon wafer is subsequently removed using a combination of grinding and selective dry etching that leaves the GaN epilayers flipped, exposed, and mounted on top of the sacrificial carrier. Following the dry etch, the exposed buffer-layer surface is rinsed in de-ionized water and a dielectric layer is immediately deposited after which the structure is ready to receive the diamond. The flipped GaN structure is schematically shown in Fig. 3 step (b). A photograph of a flipped GaN wafer is shown in Fig. 4. Finally, we attach a CVD diamond wafer to the flipped GaN epilayers using a 50 nm adhesion layer as shown in step (c). In the resulting structure, a thin GaN epilayer structure containing a heat source (transistor or laser active region) is disposed on a highly thermally-conductive diamond substrate, separated only by a thin dielectric adhesive layer. The adhesive layer presents a heat barrier with not more than 0.2 °C temperature drop when uniform power dissipation is 10 kW/cm².

3.2. Scaling the process: managing the accumulated stresses

Inasmuch as GaN and CVD diamond used in this process can both be grown on silicon, the process, in-principle, can be scaled to wafers of any size. However, due to the high-temperature steps employed during the *double flip* process, significant levels of stress accumulate in the silicon and diamond wafers. The accumulated stress can cause the wafer to crack and break during the GaN-on-diamond formation process, and severely limit the maximum achievable wafer diameter. To increase the wafer diameter we must carefully manage the stress that accumulates in the composite wafers at every step of our process.

3.2.1. Stress due to CTE

The GaN-on-diamond wafer formation process involves several high-temperature steps. Bonding the sacrificial silicon wafer to the GaN HEMT epilayers and the subsequent bonding of the diamond to the back of the GaN HEMT epilayers are both performed at elevated temperatures exceeding 700 °C. Furthermore, high temperature device fabrication steps, such as, contact annealing, require that the GaN-on-diamond wafer remains stable at temperatures exceeding 800 °C. The coefficient of thermal expansion (CTE) of silicon, gallium nitride, and diamond are distinctly different: 2.6 ppm/K for silicon; 5.6 ppm/K for gallium nitride; and ~1.1 ppm/K for diamond. Naturally, the differences in the CTE create stress in the attached wafers. The stress bows and/or warps the wafers as they cool down from the attachment temperature to room temperature. In some cases, the stress is high enough to fracture the wafers.

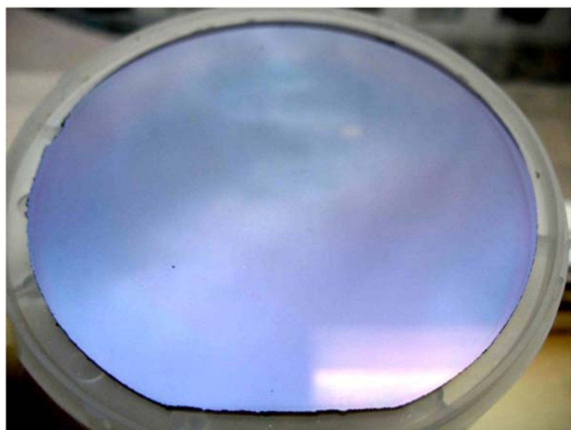

Fig. 4. Photograph of a 4-inch wafer at step (b) in Fig. 3.

3.2.2. Definition of bow/warp

We use the word *bow* to define radially uniform deflection that deforms a disk into a right-side up or upside-down bowl-like shape. Thus, when a bowed wafer is placed on a flat surface its edges touch that surface while the center is elevated by an amount equal to the total deflection of the wafer. We use *warp* to define a deformation that is an asymmetric twist or a localized deformation developed in surface that was originally flat or bowed. A warped wafer may look like a potato chip and when placed on a flat surface, it may not come in contact with the surface on its periphery. Both bow and warp can be quantified by measuring the deviation from the flat surface on which the wafer is placed. An arbitrary deformation (warp) of a disk may be described using a complete set of surface harmonics. Bow is described with the first order solution, it is radially symmetric and linear strain theory expects it to be a part of a spheroid. We will refer to the difference between warp and bow as “bow deviation”.

3.2.3. Bow and warp lead to wafer breakage

Wafer bow or warp can lead to breakage. We observed that wafer breakage is initiated at locations with material non-uniformity or edge and bulk defects. These non-uniformities concentrate the strain and can act as starting points for fissures that lead to fracture. The non-uniformities or defects can be caused by trapped debris between bonded wafers, chipped wafer edges, or even by the warp of the original GaN-on-silicon wafer that is transferred during the bonding steps. The most common step in which fracture occurs is the cool-down after diamond attachment to the flipped GaN-on-silicon, step (c) in Fig. 3.

To illustrate the level of accumulated strain in the wafers after the cool-down from diamond attachment step, consider Fig. 5. This figure shows bow measurements as a function of temperature for a 2-inch silicon-GaN-diamond just prior to the removal of the sacrificial silicon wafer. In Fig. 5, the temperature has been varied from room temperature to above 200 °C. The multiple measurements represent different wafers, all of which have nominal diamond thickness of 100 µm. It should be noted that our calculation of the bow reported in Fig. 5, is based only the linear expansion/contraction

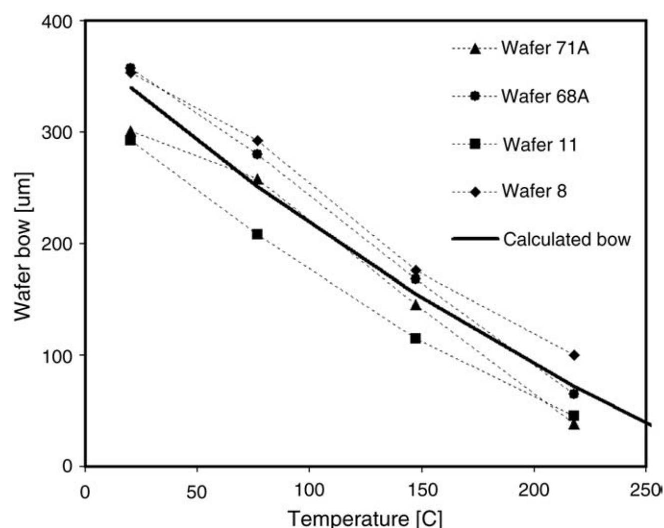

Fig. 5. Measured bow of a 2-inch silicon GaN-on-diamond wafer as a function of temperature.

Please cite this article as: D. Francis, et al., Diam. Relat. Mater. (2009), doi:10.1016/j.diamond.2009.08.017

due to varying temperature and does not include strain. Additionally it is important to note that the 300-micron bow over a 2-inch wafer is substantially larger than typical bow of a silicon wafer observed during standard commercial process (e.g. 20 µm or less). With twice the perimeter and four times the area, the scale-up from 2 to 4-inch diameter results in a higher probability for development of fracture initiation points and wafer breakage. Consequently, the 4-inch scale-up necessitates some modification of the fabrication process to further reduce the formation of non-uniformities and defects in the substrates.

3.2.4. Avoiding fractures in 4-inch wafers

Due to the increased sensitivity of our process to non-uniformity and defects, we must look for their potential cause in our *double flip* process and eliminate them. We have found that the sources of non-uniformity and defects are: (1) strain in the GaN-on-silicon epi wafers; (2) additional stress caused by adhesion layer(s) used in the *double flip* process; and (3) defects created in the carrier silicon wafer during transfer of the GaN epi. It must be noted that the magnitude of the intrinsic strain in the diamond substrate is largely managed during the diamond growth step (the discussion of this process is beyond the scope of this publication).

With respect to the first source of defect formation, the strain in the GaN-on-silicon epi is directly transferred from the growth substrate to the flipped GaN-on-carrier as shown in step (b) Fig. 3. The only caveat is that the strain is now in the reverse direction. With respect to the second cause, the adoption of an intermediate adhesion layer, would invariably add stress to the flipped GaN-on-carrier wafer. The adhesion layer improves our yield, but it also increases sensitivity to the warp of the as-grown GaN-on-silicon. Lastly, defects in the carrier silicon could be created by the removal of the growth silicon wafer; a combination of grinding and etching. These two steps can result in chipping of the edge in the carrier wafer which act as localized stress release points and can be responsible for later fractures.

With better understanding of the possible root causes of wafer fractures, we needed the ability to detect such defects to eliminate them from our process. To do this, we use bow and warp measurements of the GaN-on-silicon wafer at step (b) as an indicator of the subsequent localized strain that could lead to possible fracture of the wafer during cool-down. The bow (and warp) measurements are performed by using a Flexus non-contact surface profilometer. The measurements and subsequent analysis involves fitting of the bow profile to a quadratic function (spherical concave or convex shape expected by linear strain theory) and then evaluating the deviations from that quadratic average bow. Fig. 6(a) shows a typical measurement of the bow (height variation) and Fig. 6(b) shows the extracted bow deviation — the difference between the quadratic bow and the actual surface height variation. Such bow deviations are caused by non-uniformities in the GaN epilayers and the bonding materials.

We have found that if the magnitude of non-uniformity induced deflections from the expected CTE-induced bow exceed 10 µm in either direction, the wafers will be exposed to stress that will significantly increase the probability of fracture during cool down from the diamond attachment step at stage (c). Using this specification, we are able to get complete transfer of the HEMT film from silicon to the diamond with yields as high as 80%. Fig. 7 shows examples of several completed GaN-on-diamond wafers (including a 4-inch diameter wafer). Using the described process we can produce free-standing GaN-on-diamond wafers with bow values of less than 100 µm.

Total bow value of 100 µm, while significantly better than what has been achieved in the past, still does not meet the requirements of optical lithography for GaN-HEMT gates. This problem is alleviated by mounting the GaN-on-diamond wafer on temporary carrier which is removed at the end of the device fabrication process. Detailed descriptions of the carrier process will be the subject of future publications.

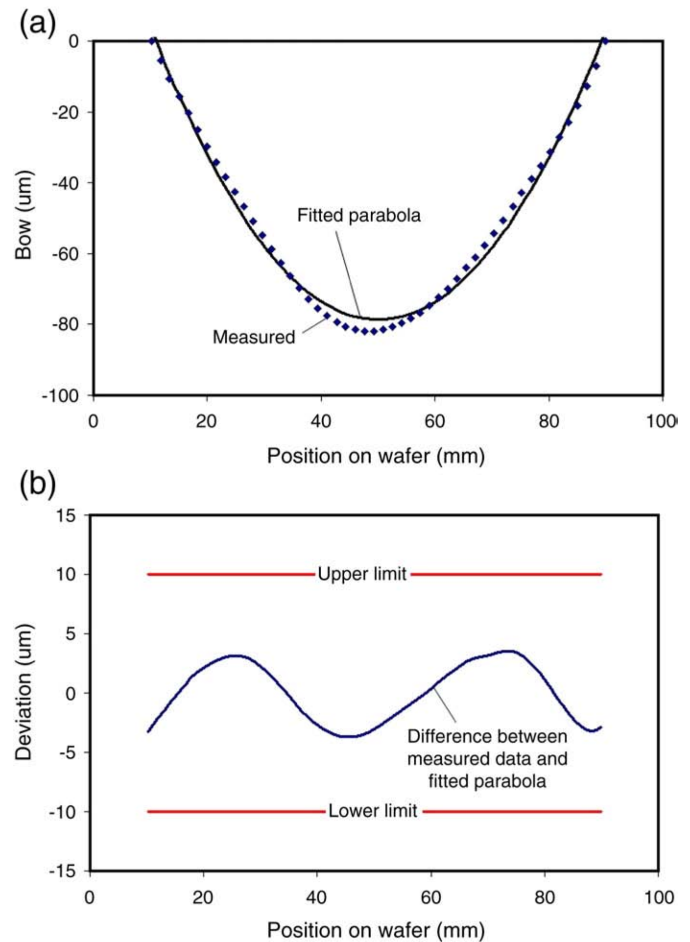

Fig. 6. (a) Measurement and parabolic fit to wafer surface profile data, and (b) deviation from quadratic behavior (warp) with limits that ensure wafer integrity — no fractures.

4. Description of the GaN-on-diamond interface characterization

Maintaining high thermal conductance of the interface between CVD diamond and GaN epilayers in the direction perpendicular to the interface is essential to make GaN-on-diamond a viable thermal-management technology. This means that the interface must exhibit good adhesion properties and high bond strength. We characterized the acoustic properties of the layered structure, including GaN and diamond, using picosecond laser-ultrasonic probing. This technique,

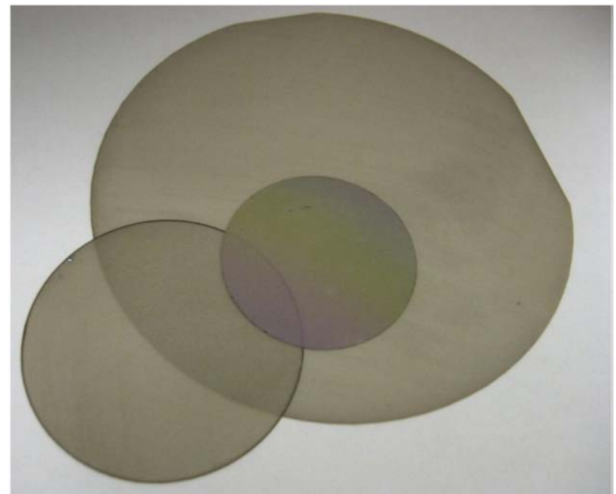

Fig. 7. Several GaN-on-diamond wafers.

Please cite this article as: D. Francis, et al., Diam. Relat. Mater. (2009), doi:10.1016/j.diamond.2009.08.017

described in detail in reference [14], is based on placing a photon-to-phonon transducer on top of the layer structure to be studied and is referred to as an acoustic phonon echo technique. The technique uses very short light pulses to generate longitudinal phonons that reflect off of the layer interfaces in the structure. The reflected signal depends on the acoustic properties of the materials and the interfaces. The analysis of sound velocity, attenuation, and the discontinuities in such signals can reveal slippage or poor adhesion. Using the acoustic phonon echo technique, we measured our GaN-on-diamond samples to characterize adhesion of the GaN to the diamond and the acoustic properties of the interface material.

The cross-section schematic of the measured sample is shown in Fig. 8. The structure comprises of a 100-micron thick CVD diamond substrate with a 50-nm proprietary adhesion layer, and a 2-micron thick GaN epitaxial structure. The GaN epitaxial structure contains the 2D electron gas. A 140-nm thick aluminum layer is deposited on top of the GaN epilayers to serve as the photon-to-phonon transducer. Through the acoustic phonon echo technique, sub-picosecond light pulses hit the transducer and set up thermal stress that launches ultra-short photon pulses into the GaN layer. When these pulses reach the bonded interface, they are partially reflected. The shape of the returning sound echo is dependent on the acoustical properties and the thickness of the bonding layer and can also show additional structure if the adhesion between the layers is imperfect. We determined the properties of the interface using a simulation which calculates the shape of the echo for arbitrary properties of the bonding layer. We varied the thicknesses of the GaN and the bonding layer as well as the longitudinal sound velocity in the adhesion layer as inputs to the model until the calculated response matched the measured response. The first returning echo from the GaN/diamond interface (shown in Fig. 9) has been fit to a model by treating the thickness of the Al, the GaN, and the interface dielectric layers as adjustable parameters. The sound velocity in GaN is taken as 8.0 nm/ps and in diamond 20.0 nm/ps. Best fit parameters are $d_{Al}=$ 140 nm, $d_{GaN}=1835$ nm, and $d_x=51$ nm. The fitting has been based on perfect mechanical bonding at the interface with a single homogenous layer of interface material. We also assumed that there is no attenuation of sound in the GaN. If significant attenuation were present, it would wash out the fine structure in the echoes — this has not been observed. Fig. 9 shows the match between the measured and calculated echo responses from GaN-on-diamond interface of the 4-inch wafer shown in Fig. 7. The results show a remarkably good fit that places the bonding layer thickness d_x at 51 nm and indicates excellent adhesion between all of the layers. We will provide a characterization of the interfacial thermal resistance in a future publication.

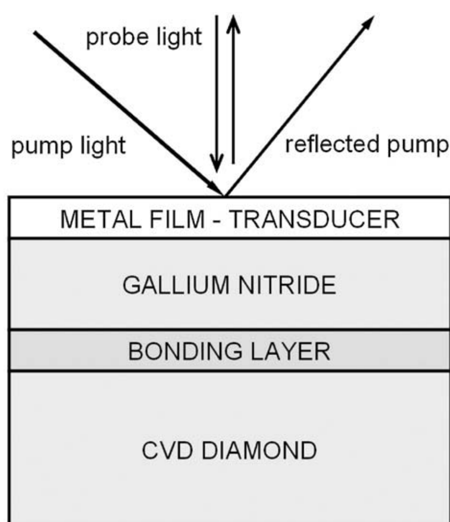

Fig. 8. Cross-sectional view the sample used in picosecond ultra-sonic measurement.

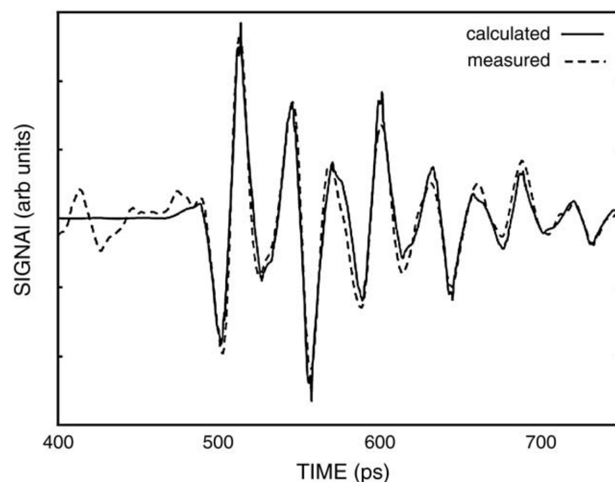

Fig. 9. Measured and modeled ultra-sonic echo comparison.

5. Conclusion

We have successfully demonstrated 4-inch, 100-micron GaN-on-diamond wafers. The choice of the diamond thickness is targeted toward the typical GaN HEMT size. The analysis of the interface shows GaN to be well attached to the diamond.

Our reports on working GaN-on-diamond devices fabricated on wafers prepared through the process herein described are published elsewhere [15]. The device results attest to the quality of the GaN-on-diamond engineered wafers. A comparison between device performance between GaN-on-silicon and GaN-on-diamond reported in reference [15] confirms that the double-flipping and bonding processes do not introduce any damage to the active epilayers. The record high frequency performance of GaN-on-diamond HEMTs with $f_T=$ 85 GHz is reported in reference [16]. These developments put the GaN-on-diamond technology on the path to commercialization in high-power, high-frequency amplifiers.

Acknowledgement

The authors acknowledge the Air Force Research Labs (Phase III) SBIR contract #FA8650-09-C5404 and Missile Defense Agency (J. Blevins) contract #HQ0006-07-C-7654 for support of this work.

References

[1] L.F. Eastman, U.K. Mishra, IEEE Spectrum (May 2002) 28.
[2] U.K. Mishra, P. Parikh, Y.-F. Wu, Proc. IEEE 90 (2002) 1022.
[3] R. Quay, Gallium Nitride Electronics, Springer-Verlag, Berlin Heidelberg, 2008.
[4] S. Nakamura, S. Chichibu (Eds.), Introduction to Nitride Semiconductor Blue Lasers and Light Emitting Diodes, Taylor and Francis, London New York, 2000.
[5] D. Francis, J. Wasserbauer, F. Faili, D. Babić, F. Ejeckam, W. Hong, P. Specht, E.R. Weber, GaN HEMT Epilayers on Diamond Substrates: Recent Progress, Proc. CS MANTECH, Austin, TX, 14–17: May, 2007.
[6] P.R. Hageman, J.J. Schermer, P.K. Larsen, Thin Solid Films 443 (2003) 9.
[7] P.W. May, a.H.Y. Tsai, W.N. Wang, J.A. Smith, Diamond Relat. Mater. 15 (2006) 526.
[8] M. Oba, T. Sugino, Diamond Relat. Mat. 10 (2001) 1343.
[9] G.W.G. van Dreumel, J.G. Buijnsters, T. Bohnen, J.J. ter Meulen, P.R. Hageman, W.J.P. van Enckevort, E. Vlieg, Diamond Relat. Mat. 18 (2009) 1043.
[10] J.W. Zimmer, Mater. Res. Soc. Symp. Proc. 956 (2007).
[11] E. Piner, J.W. Zimmer, J.C. Roberts, G. Chandler, R.A. Sadler, Extended Abstracts 33rd WOCSDICE, Málaga, Spain session Mon4-Diamond, 2009, p. 18.
[12] P. Hui, H.S. Tan, Jpn. J. Appl. Phys. 35 (1996) 4852.
[13] A. Rogacs, J. Rhee, IEEE Adv. Packaging Materials Symposium, 2007, p. 65.
[14] C. Thomsen, H.T. Grahn, H.J. Maris, J. Tauc, Phys. Rev. B34 (1986) 4129.
[15] J.G. Felbinger, L.F. Eastman, J. Wasserbauer, F. Faili, D.I. Babić, D. Francis, F. Ejeckam, Extended Abstracts 33rd WOCSDICE, Málaga, Spain, session Mon4-Diamond, 2009, p. 22.
[16] Q. Diduck, J. Felbinger, L.F. Eastman, D. Francis, J. Wasserbauer, F. Faili, D.I. Babić, F. Ejeckam, Electron. Lett. 45 (2009) 758.

Please cite this article as: D. Francis, et al., Diam. Relat. Mater. (2009), doi:10.1016/j.diamond.2009.08.017