# AlGaN/GaN HEMT on Diamond Technology Demonstration

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### Abstract

*This letter is a first report on the operation of AlGaN/GaN high-electron mobility transistors (HEMTs) atomically attached to a CVD diamond substrate. This technology demonstration shows the feasibility of producing GaN based devices on polycrystalline CVD diamond substrates to maximize heat extraction from devices operating at high power by situating the diamond substrates in the immediate proximity of the transistor channel. Such an approach offers tremendous opportunity for efficient and effective heat management of high power devices. We demonstrate the ability to preserve the electrical properties of AlGaN/GaN HEMTs throughout the GaN-on-diamond atomic attachment process and report on the fabricated DC and small-signal HEMT characteristics.*

### Keywords

GaN, high electron mobility transistor (HEMT), diamond, power, wafer bonding.

## INTRODUCTION

AlGaN/GaN device applications are designed for use at very high power densities compared to any other existing device technologies [1-3]. While the AlGaN/GaN materials can sustain operation at high power densities due to an exceptionally high breakdown voltage, existing heat-extraction technology limits the maximum achievable power density from GaN materials: gallium nitride and common low-cost substrates used for its growth (e.g. silicon, sapphire) have poor thermal properties. For this reason, numerous approaches have been explored to improve the thermal management of such devices [4-6]. The difficulty with many of these techniques is that in all semiconductor devices due to their size, the largest temperature drop occurs in the immediate proximity of the device where the heat flux is the highest. Therefore, any efficient thermal management approach must reduce the thermal resistivity of the materials and/or spread the heat flow in the immediate region of the heat source: immediately below and above the channel of the field-effect transistor and the ohmic contacts. Synthetic diamond heatsinks have been used successfully in the industry for spreading the heat and lowering the temperature of entire chips [7]. However, the full advantage of the diamond's thermal conductivity (three times that of silicon carbide) has never been fully utilized because heat spreading of entire chips places the diamond substrate at a distance from the heat source of several tens or hundreds of micrometers which is many times larger than the device feature size. The device features are on the order of several micrometers (field-effect transistor channels and current crowding hotspots). By placing the diamond heatsink to within a few microns of the heat source (or less), the temperature increase at the device level can be substantially mitigated; this solution fully exploits diamond's high thermal conductivity leading to a dramatically lower thermal resistance in high-power devices.

We report on a HEMT in which the diamond substrate is situated 1.2 μm below the electron channel. The HEMT was fabricated by first transferring the device active layers from a silicon substrate on which they were originally grown to a chemical vapor deposited (CVD) diamond substrate. Subsequent to the layer transfer, the device was fabricated atop the diamond substrate. A proprietary process developed by Group4 Labs (Group4) was used to transfer and attach the gallium nitride materials to polycrystalline CVD diamond substrates. The novel HEMT structure thus allows heat extraction directly from the channel. The projected reduction in operating temperature will come from i) the superior thermal properties of diamond (i.e. 1200 W/m/K compared to 400 W/m/K for SiC) [4], and ii) the close proximity of diamond to the channel. In this letter, we show the first fabricated GaN-on-Diamond FET technology demonstration as feasibility of the integrated heat-sink concept for use in many types of device applications. These GaN-on-Diamond structures can then be mounted on a larger heat-sink for maximum thermal dissipation.

## FABRICATION AND MEASUREMENTS

The devices used in this experiment were grown by metal organic chemical vapor deposition (MOCVD) on Si (111) substrates. The epilayers structure starting with the silicon substrate consists of an AlN nucleation layer, a 1.3 μm undoped GaN buffer layer, a thin AlN interlayer, a 18.5 nm $Al_{.27}Ga_{.73}N$ barrier layer and a thin GaN cap layer. The finished epi surface is free of surface cracks with a sheet resistance uniformity of 3.9% across 2" wafer. The sheet charge density is 9.1 x$10^{12}$ $cm^{-2}$ with a pinch off voltage of 3.7 V, measured by Hg probe C-V test.

Following the growth, the AlGaN/GaN/Si wafer was coated with 2300 Å $SiN_x$ and frontside-mounted to a mechanical substrate. The Si substrate was then removed from the backside to reveal the GaN buffer layer which was then atomically attached to a flat 25-µm thick polycrystalline CVD diamond substrate. Fig. 1 shows a schematic of the layer structures up to this point. After the attachment process, the mechanical substrate is removed from the front side. The structure is then backside mounted to a Si carrier wafer using a high temperature glass adhesive layer for device fabrication (diamond substrate to silicon carrier). This last attachment process is not ideal. The high-temperature glass adhesive and the silicon substrate add thermal resistance to the device and mask the benefits of thermal resistance reduction that would be realized if the diamond substrate was mounted directly to a copper block. The last attachment process to Si was used to fabricate HEMTs and demonstrate that the layers would survive the diamond bonding process. Future iterations will involve mounting the diamond layer directly to thermally conductive packaging. Fig. 2 shows the resulting AlGaN/GaN/diamond stack. The quality of the atomic bonding process is evident.

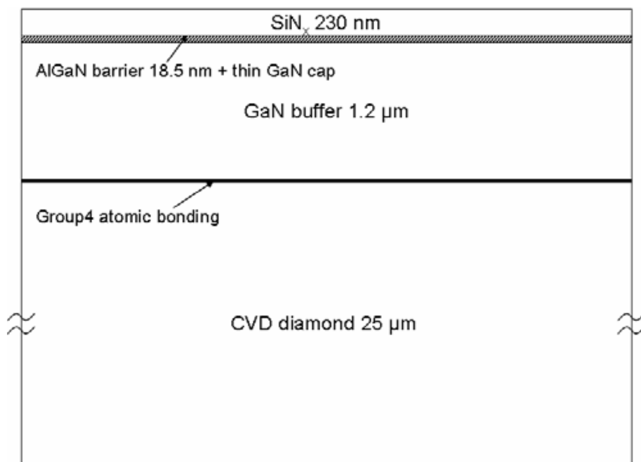


**Figure 1. Schematic diagram of active layer with growth substrate removed and bonded to the CVD diamond layer. The surface is covered with $SiN_x$.**

The HEMTs were fabricated using the standard quick-lot GaN device process at AFRL. The device fabrication process was not optimized for this particular source of material. The protective $SiN_x$ layer was removed with a $CF_4/O_2$ RIE etch. Mesa isolation was performed with a two-step $Cl_2/BCl_3/Ar$ ICP etch followed by $Cl_2/Ar$ RIE etch to 500 Å. Ohmic contacts were formed with Ti/Al/Ni/Au (350/2333/500/200 Å) annealed at 850 ºC for 30 seconds in a nitrogen ambient. The source-drain spacing of these devices was 4.5 µm. Optically defined 1.5 µm gates were formed with Ni/Au (200/3800 Å). The total gate periphery is 2x150 µm. No pre-metal surface clean was used, and the devices were not passivated.

DC and RF characterization was performed on process control monitor (PCM) structures and the optically defined devices. PCM structures were measured on a Keithley 450 with a standard 24 pin probe card. DC data was taken with an HP4142. Small signal s-parameters were measured from 1 GHz to 26 GHz with an HP8510 vector-network analyzer and Cascade Microtech on-wafer probes. Frequency response was determined from extrapolating the $h_{21}$ and frequency product for each frequency to the single pole unity current gain and taking the average.

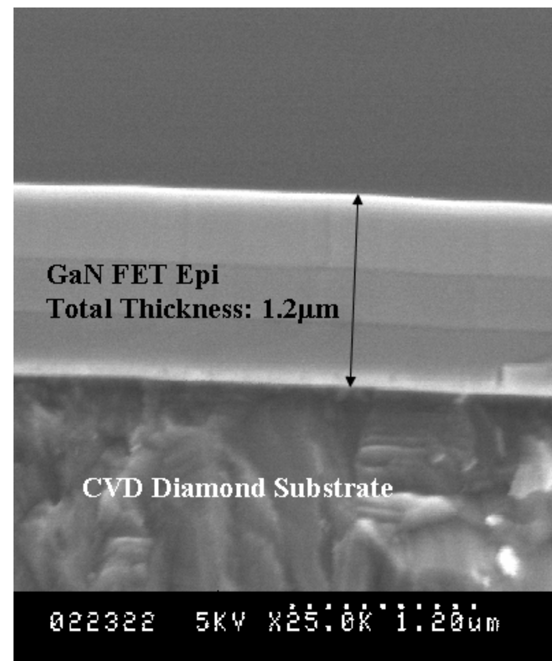


**Figure 2. SEM cross section of AlGaN/GaN atomically attached to CVD diamond. The buffer layer is in direct contact with the diamond.**

## RESULTS AND DISCUSSION

Transfer length method (TLM) measurements of the wafer show high contact resistance values of 6.09 ± 0.41 Ω•mm. The contact resistance values are high because the ohmic contacts used were not optimized for this particular source of epi. The sheet resistance of this sample was measured at 476 ± 30 Ω/sq with the same TLM measurements. This value compares well with the Lehighton measurement performed on diamond bonded wafer (412 Ω/sq) prior to device process indicating that the 2-DEG interface remains intact after the bonding process. Isolation voltage measurements across a 5 µm gap between mesas exceed 60 V compliance at 10 µA for all sites measured. This indicates that the buffer remains insulating after the bonding

and fabrication processes and is suitable for device applications.

Fig. 3 shows DC I-V curves of the device with $V_{GS}$ stepping from +1.0 to –3.0 V in 1.0 V increments. The drain voltage is swept out to 20.0 V. The reduction of drain-current characteristics with increasing $V_{DS}$ has a strong contribution from heating caused by the increased thermal resistance of the thinned substrate mounted to the silicon carrier by the glass adhesive. The knee voltage is high and the drain current is low due to large contact resistance values. The DC I-V curves do not show typical dispersion characteristics seen in other unpassivated devices. Instead, the unpassivated curves are relatively smooth.

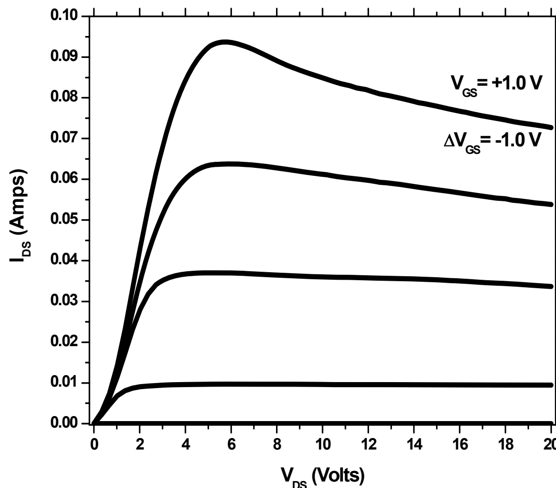


**Figure 3. Drain current-voltage characteristics for unpassivated 1.5x2x150 μm GaN-on-diamond HEMT.**

Fig. 4 shows the transfer characteristics of the same device with $V_{DS}$ = 5.0 V to maximize the gain. The gate voltage is swept from -5.0 to +1.0 V for the forward sweep and back from +1.0 to -5.0 V for the reverse sweep. The hysteresis in the forward and reverse curves indicates dispersion effects. These effects are not well understood for this particular process, but there have been numerous reports on hysteresis and surface trapping effects in unpassivated GaN FETs. They are typically attributed to virtual gate formation due to surface charging [8-11]. These effects will most likely be removed by subsequent iterations and $SiN_x$ passivation of the devices.

The measured device parameters include: $g_{m\text{-}peak}$ = 70 mS/mm, $f_T$ at $g_{m\text{-}peak}$ = 8.0 GHz, $f_{max}$ (MAG) at $g_{m\text{-}peak}$ = 11.4 GHz, $V_{TH}$ = -2.9 V, $I_{DSS}$ = 283 mA/mm, and $I_{max}$ = 306 mA/mm. These measurements were taken at $V_{DS}$ = 5.0 V with $I_{DSS}$ and $I_{max}$ at $V_{GS}$ = +1.0 and 0.0 V respectively. The low current is due to the high ohmic contact resistance. The $f_T$*$L_G$ product of 12 GHz•μm is in agreement with other device quality AlGaN/GaN materials that we have processed indicating promise of good device performance with process optimization.

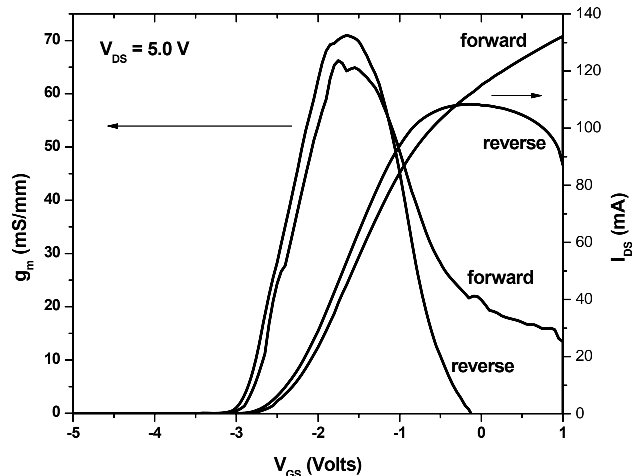


**Figure 4. Transfer characteristics of the same device with drain biased at 5.0 V. Forward and reverse gate sweep shown.**

## CONCLUSION

We have demonstrated the first successful HEMT fabrication using a GaN-on-Diamond atomic attachment technology. This integrated heat-sink capability is expected to enable very high power density operation due to improved packaging and heat extraction. Our work shows that the GaN materials and the 2DEG remain intact during the substrate transfer and atomic attachment to diamond heatsinks. We expect that further process improvement, mounting techniques, and process optimization should yield high performance devices with very high power operation.

## ACKNOWLEDGMENTS

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