GaN-on-diamond Field-Effect Transistors: from Wafers to Amplifier Modules

D. I. Babić[1], Q. Diduck[1], P. Yenigalla[1], A. Schreiber[1], D. Francis[1], F. Faili[1], F. Ejeckam[1], J. G. Felbinger[2], L. F. Eastman[2]

[1]Group4 Labs, Inc., 13500 Stevenson Place, Suite 207, Fremont, CA 94539, USA

[2]Cornell University School of Electrical and Computer Engineering, Ithaca, NY 14853, USA

Phone: (408) 398-2484 Fax: (408) 689-9674 E-mail: dubravko.babic@group4labs.com

Abstract—We describe the development and issues related to fabrication, die processing, and packaging GaN-on-diamond high-electron mobility transistors into X-band amplifier modules. We perform thermal resistance measurements on these amplifiers using liquid-crystal thermography and show that they agree with theory and previously published measurements on GaN-on-diamond devices.

I. INTRODUCTION

Thermal management is an essential element of successful design of high-performance electronic power devices. Over the past decade, the commercial availability of gallium-nitride (GaN) electronic components such as field-effect transistors, Schottky diodes, light-emitting diodes, and lasers has made profound impact on consumer, professional, and military electronics [1,2]. High-power RF electronics based on GaN are actively being investigated by chip manufacturers for replacement of silicon LDMOS and GaAs pHEMTs in wireless and microwave communication systems and commercial phased-array radar. Manufacturers of radar, deep-space, and military communication equipment are seeking to enhanced or replace travelling-wave tube amplifiers using solid-state components where GaN stands as the top choice. The reason for such high interest lies with the electrical properties of GaN and related components (AlGaN, InAlN). They exhibit a combination of key material parameters that is better than any other material used in RF power and switching: higher breakdown field, electron channel density, and mobility. Table I illustrates the comparison between the material properties of Si, GaAs, SiC, GaN using Power-Frequency Figure of Merit (PFFM $P_{\max} f_T \propto (E_C v_s/2\pi)^2$) derived from Johnson [3] and Baliga High-Frequency Figure of Merit (BHFFM $1/R_{SP}C_{SP} \propto \mu_e E_C^2$) from Baliga [4] relative to silicon. The availability of high-quality AlGaN compounds and two-dimensional electron gas makes GaN significantly more versatile material than silicon carbide, its main competitor for high power applications.

TABLE I
MATERIALS USED FOR RF POWER TRANSISTORS

Material	E_{CRIT} MV/cm	μ_e cm²/Vs	κ (300K) [W/cmK]	BHFFM	PFFM
Si	0.3	1350	1.5	1	1
GaAs	0.4	8500	0.46	16	11
4H-SiC	3	700	4.5	34	410
GaN	3.3	1800	1.3	100	790

Owing to its high maximum drain current and operating voltages, GaN HEMTs can exhibit output powers greater than 10 W/mm of gate periphery (at X-band) which is more than an order of magnitude higher than that of GaAs pHEMT. Furthermore, relative to the GaAs pHEMTs, GaN HEMTs exhibit lower input capacitance and higher output impedance for the same power, while higher output power per unit gate periphery reduces the need for on-chip power combining – a source of reduced amplifier efficiency. These numbers show that GaN is truly a wonder-material.

However, there is a downside: heat conductivity of GaN and related compounds are lower than that of silicon. Furthermore, the substrates on which the GaN devices are commonly grown, sapphire and silicon have low thermal conductivity much lower than that of SiC and chemical-vapor deposited (CVD) diamond. Although some RF power devices are commercially fabricated on SiC substrates, their output power and efficiency can be improved further by placing GaN epilayers on CVD diamond. This is particularly important for devices that have inherently small features yet process large power densities, such as, high-power RF and millimeter-wave transistors and single-mode visible semiconductor lasers. For this reason, there has been a substantial effort in the industry to integrate GaN with synthetic diamond [5, 6, 7, 8, 9,10].

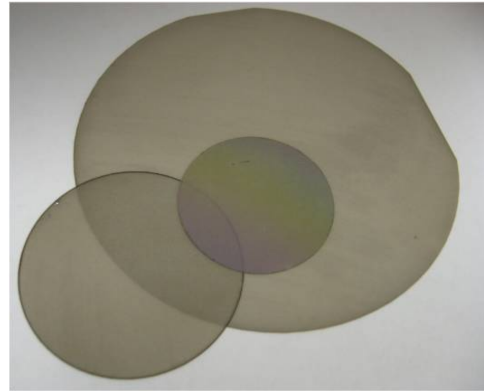

Fig. 1 GaN-on-diamond wafers

We have invented and developed a process that profoundly expands GaN chip thermal properties [11,12]. In this process, a GaN epilayer is atomically attached to chemical-vapor-deposited (CVD) diamond wafer creating an engineered wafer with GaN-based active layers disposed on a CVD diamond substrate (see Fig. 1). Using this technology, we have successfully demonstrated high-electron mobility transistors (HEMT) with f_T ~ 85 GHz [13] and 4 W/mm output power [14], full wafer processing [15], and have demonstrated that the thermal resistance of GaN-on-diamond transistors is half that of similar transistors on silicon carbide [16].

Lowering the thermal resistance of power devices has numerous advantages: (a) Out of two devices operated at a fixed ambient temperature, the one with lower thermal

resistance will have lower channel temperature and consequently will be capable of delivering more output power, at a higher power-added efficiency, and will experience longer mean-time-to-failure (MTTF). (b) Maintaining the channel temperature at a specified level, typically 150°C, the device with lower thermal resistance will deliver equal output power, efficiency, and MTTF at a higher ambient temperature. This is very important as allowing higher ambient temperature means reduced cooling costs, or in some cases a significant change in the cooling approach (e.g. replacing water cooling with air cooling). (c) Ultimately, chips can be made smaller thus reducing the cost, while still improving their thermal resistance.

The reduced thermal resistance in GaN-on-diamond electronic devices stems from highly efficient heat spreading: the device active region (i.e., field-effect transistor conductive channel) is placed in the immediate proximity of a highly thermally conductive substrate. In our case, the body of the chip is made out of diamond and the heat is generated less than two micrometers away from it. Our next-generation process will reduce this distance even further. In field-effect transistors and Schottky diodes the heat is generated along narrow strips concentrated near the gate edge of gate-to-drain regions of field-effect transistors and anode-to-cathode strips of Schottky diodes. Due to concentrated heat flow, it is in these regions that the one observes the largest temperature rise in packaged devices. By placing diamond to within a micrometer of the heat source we affect the heat flow in the most critical location of the device and experience highest impact on the overall device thermal resistance. This is most clearly observed on measurements in which we compared GaN/SiC and GaN-on-diamond HEMTs [16] and found that GaN-on-diamond HEMTs operate at half the junction temperature of the GaN/SiC HEMT. This fact has far-reaching consequences on RF and millimeter-wave MMIC design as shown in Fig. 2 where we compare the expected thermal resistance of GaN-on-diamond chips with commercially available X-band field-effect transistors and MMICs based on GaN/SiC HEMTs and GaAs-pHEMTs. The thermal resistance of power MMICs is primarily determined by the lateral size of the output transistor, the physical size of the transistor in the direction perpendicular to the gate fingers (lateral size includes gate pitch and source-to-drain spacings). In Fig. 2, we plot the thermal resistance versus the transistor lateral size for transistors with 125-μm unit gate width (typical for X-band). The key facts shown in Fig. 2 are that GaN-on-diamond devices offer an order of magnitude lower thermal resistance than GaAs pHEMT and a factor two lower thermal resistance than GaN/SiC devices for the same transistor lateral size and, consequently, same chip size.

In this paper, we describe the development of the first RF power amplifier modules based on GaN-on-diamond HEMTs operating in the X-band; we describe the complete process sequence starting with the engineered GaN-on-diamond wafers and ending with a connectorized amplifier module. The purpose of this work is to be present an overview of the different technologies needed to develop RF GaN-on-diamond amplifiers.

Developing high-frequency solid-state amplifiers in GaN-on-diamond technology is challenging: (a) Diamond is the hardest material known to man and diamond substrates are difficult to micro-machine; wafers cannot be diced using traditional methods usually applicable to silicon (Si) and other compound semiconductors. (b) Wafer thinning, although possible, is impractical primarily because diamond substrate cost is proportional to its thickness—one would not want to remove material that was quite costly to create. (c) The most significant consequence of the fact that diamond wafer cost scales with its thickness is that the GaN-on-diamond wafer thickness (selected prior to device fabrication) becomes the final thickness of the completed chip. For monolithically integrated microwave integrated circuits (MMICs) chip thicknesses range between 50 and 100 μm. Most commercial foundries are not equipped to handle wafers thinner than several hundred micrometers because such free-standing wafers are fragile and can exhibit unacceptably high bow. Commercially lithography tools, contact lithography and especially e-beam are intolerant of wafer bow and maintain stringent bow specifications (e.g., less than 50 μm deviation on a 100 mm wafer). To address this difficulty, we have developed a Si-wafer carrier to enable processing of GaN-on-diamond wafers in existing commercial foundries [17]. In this paper we discuss processes and devices developed on free-standing 15 x 15 mm² samples.

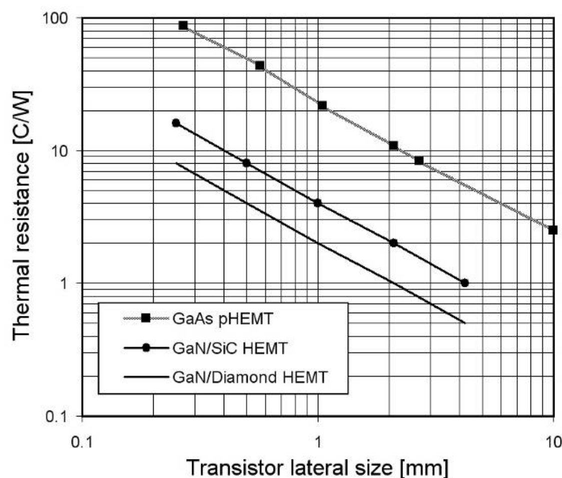

Fig. 2 Comparison between the thermal resistance of typical commercially available X-band MMIC amplifier chips based on GaAs p-HEMTs and GaN/SiC relative to GaN-on-diamond.

II. Wafer, Device Design, Fabrication and Characterization

The process of transferring GaN epilayers to diamond starts with a GaN/Si wafer which contains the finished HEMT epilayers. The epilayer structure of the future HEMT is thus defined at the beginning of the process, before the attachment to diamond. Various structures can be implemented according to the specification of the final engineered-wafer customer. The HEMT epilayer structure is typically grown by metal-organic chemical-vapor deposition (MOCVD) on (111) Si substrates. In this work, the epilayer structure consisted of a manufacturer-proprietary nucleating layer followed by an 800-nm unintentionally doped (UID) GaN buffer layer and a 17.5 nm $Al_{0.26}Ga_{0.74}N$ barrier layer which was capped with 2 nm UID GaN [18]. This epilayer stack was first attached (face to face) to a sacrificial substrate and its growth (111) Si substrate is removed. Next, the exposed back of the GaN stack was atomically attached to a 100-μm thick chemical-vapor deposited (CVD) diamond substrate. This double transfer is necessary to preserve the GaN crystal orientation: Ga-face remains on

top. Fig. 3 schematically illustrates the process of manufacturing GaN-on-diamond wafers. Further details of the manufacturing of the GaN-on-diamond wafers are given in references [11,12].

The smooth surface of the diamond wafer (the mandrel face) is adjacent to the GaN/AlGaN epilayers, while the rough surface of the diamond (growth face) forms the wafer back. The diamond substrates were grown using microwave plasma and exhibit columnar-grain growth with grain size of ≈ 20 µm at the growth surface. We measured the bulk heat conductivity (average value for the entire wafer) of diamond wafers used in this work to be $\kappa_D \geq 1{,}500$ W/cmK. The thermal conductivity of CVD grown diamond increases with the diamond thickness [19]. The diamond thickness is selected to be on the order of the HEMT unit gate width based on a previous study that shows that optimal heat spreading occurs when the characteristic size of the heat source is comparable to the thickness of the heat spreader [11].

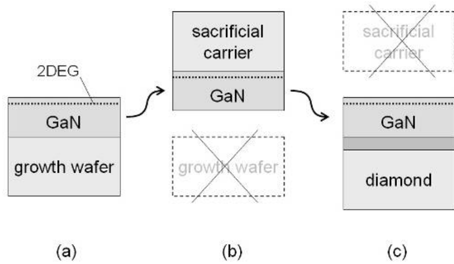

Fig. 3 Schematic diagram of GaN-on-diamond wafer manufacture

The device fabrication for this work used six e-beam lithography steps. In the future all but the gate and possibly gate recess will be performed using optical lithography. The processed devices had two gate-fingers and no air-bridges. For devices with four or more gate-fingers, air-bridges are needed and this would add two additional lithography steps. GaN-on-diamond wafer process begins with the creation of Ti-Pt alignment marks that are used for the alignment of subsequent layers and laser scribing. This is followed by ohmic metal deposition, PECVD silicon nitride passivation, mesa isolation using B/Cl_3 reactive ion etching, contact pads, and Ni/Au gates. Ohmic-contacts consisted of Ta/Ti/Al/Mo/Au metal stack. The contact anneal is performed in a nitrogen atmosphere in a two step process: 700°C/60 secs and then 800°C/20secs. The contacts and the epilayers were characterized by Transfer Length Method (TLM) measurement. Sheet resistance of 434 Ω/sq, transfer length of 0.94 µm, and a contact resistance of 0.4 Ωmm were measured. The process for bonding pads involves a separate gate metallization which uses Ti-Au metallization. No thru vias were implemented at this time. As diamond substrates are insulating, there was no need for backside contact metallization. In the future, for RF and millimeter-wave MMICs, the traces on top of the chip will use either micro-strip or conductor-backed coplanar waveguide (CB-CPW) transmission lines. All such implementations will require back-of-wafer metallization and thru-via technology.

Devices with a variety of gate lengths (100 nm, 150 nm) and gate widths (150, 200, and 300 µm) were built. Other relevant HEMT dimensions were L_{GS} = 500 nm, L_{DG} = 2 µm, gate pitch 50 µm, and the overhang (field plate) on the Γ-shaped-gate was 60 nm. A finished 2 x 150-µm device is shown in Fig. 4, with two focal depths showing the top surface of the wafer (focus on the device) and the bottom surface (focus on the diamond back surface as seen though the wafer); both AlGaN/GaN epilayer and the diamond substrate are transparent to visible light. The transistors were laid out on a 600 x 600 µm grid to avoid any e-beam stitching errors (300-µm) in a rectangular 16 x 16 array (sample wafer size 15 x 15 mm²). RF coplanar probes were used to measure small-signal *s*-parameters, source/load pull, and DC performance on the wafer.

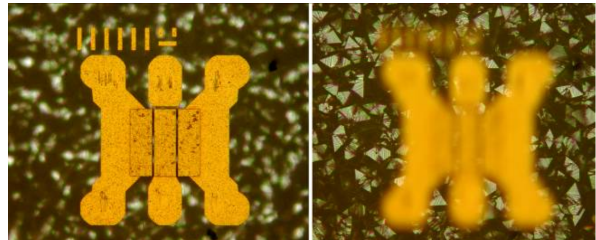

Fig. 4 Image of 2 x 150 µm HEMT with focus on the device and focus on the back of the diamond wafer showing diamond crystals on the back surface (diamond is transparent)

We made amplifiers from W_G = 2 x 100-µm devices with L_G = 100 nm gate. This decision was based on the desire to optimize gain at 10 GHz (gate width around 100 µm is typically used for negligible phase error) and shortest gate length (higher transition frequency). The average maximum drain current of 850 mA/mm was measured. This is also typical for GaN/Si HEMTs. The device breakdown voltage was > 30 V which enabled 15V operation in Class AB. Typical on-wafer-measured source/load-pull measurements are shown in Figure 5.

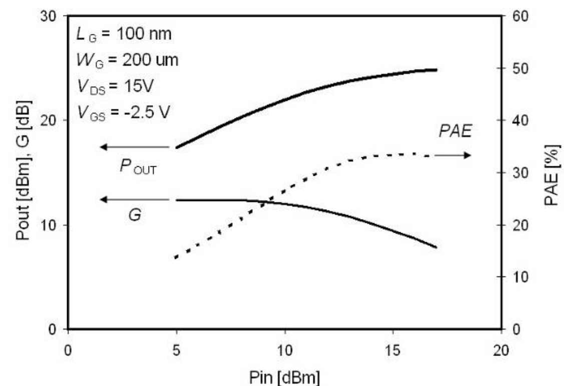

Fig. 5 On-wafer power-in/power-out measurements at 10 GHz.

III. Die Processing

In the semiconductor industry, dicing is accomplished either by sawing of the wafer or scribing and cleaving the wafer into individual die. For single-crystal wafers (silicon and GaAs, for example), scribing and cleaving traditionally means separating wafers into die along crystallographic planes that naturally have weaker bonds. CVD diamond is polycrystalline and there is no one crystallographic plane along which the crystal may break to leave a flat edge, so the weakening of the wafer has to be accomplished using laser micromachining. We scribed the GaN-on-diamond

wafers by laser-etching trenches in a rectangular 600 x 600 μm² (Manhattan) pattern. The laser-scribing is performed while the wafer is attached to standard dicing tape stretched on a hoop [20]. Figure 6 shows the side of a cleaved diamond wafer with the profile of a laser-scribe of 40-μm depth. The AlGaN/GaN epilayers constitute the top 2 μm of the wafer in Fig. 6, but cannot be resolved in this optical microscope image.

The laser drilling of diamond is a combination of thermal graphite ablation, which re-deposits graphite debris around the cut, and chemical etching in which graphite burns producing CO and CO_2 [21,22]. The balance between these two processes is determined by the average laser power and the availability of oxygen. It is of critical importance that the laser scribing be debris-free because cleaning the graphite debris from individual die is quite difficult. In order to maintain a clean cut (no graphite redeposit), we adjusted the scribing conditions to burn (chemically etch) diamond by laser-scribing in oxygen atmosphere and to keep the laser average power at a level that produces little or no debris around the cuts. Furthermore, to minimize the heat damage, which increases the scribe alley width, we maintain laser pulse duration well below the thermal time constant of diamond mass at the drilling location (estimated to be around 200 ns for a 25 μm beam spot) [23]. The typical scribing conditions on a Q-switched Nd:YAG 1064 nm laser were $P_{AVG} \leq 200$ mW, repetition frequency 1.5 kHz, beam speed 6.25 mm/s, and pulse duration: 35 ns to 60 ns [24]. Using this process we were successful in realizing 50-μm wide scribe alleys, although at least 80 μm is preferable for < 25-μm beam diameters.

Fig. 6 Side-view of a cleaved 100-μm GaN-on-diamond wafer. One un-cleaved scribe is visible; the scribe depth is 40 μm.

Wafer cleaving is done manually by pressing the dicing hoop with the blue tape against the rounded edges of a cleaving wedge. The ability to cleave a wafer using the cleaving wedge depends on the difference in torque that can be exerted on two adjacent die on the wafer. The smaller the die, the harder it is to cleave it, and no matter how thin the diamond is, this still presents a challenge. Our experience is that the ratio between the smallest die dimension and the remaining uncut thickness of diamond should be at least 15:1 for an efficient cleave. The HEMT wafers used in this work were scribed to a 60 μm depth. Diamond dust produced by the breaking of large un-scribed sections of the wafers is potential difficulty as it often lands on the surface of the die and scratches the metallization.

For final RF packaging, GaN-on-diamond chips will eventually provide a back-side contact for mounting and return path. This is planned to be accomplished with metal-coated thru vias that will connect the top source electrodes to the metalized back of the wafer using a process and recipe based on the above-described laser scribing.

IV. Amplifier Design and Build

We designed a single-stage hybrid amplifier with one HEMT mounted on a copper-clad duroid® substrate. The tuning and bias networks were placed on a microwave substrate, while the substrate is inserted either into an RF test-fixture or packaged into an in-house developed high-frequency/high-thermal-conductance package (described in the next section). The microwave substrates consist of a 125-μm thick RT/duroid® 5880 dielectric [25] with $\varepsilon_r = 2.2$ and $\tan(\delta) = 0.0009$ at 10 GHz attached to 1-mm thick copper plate, commonly referred to as "hard-clad duroid". Copper-clad duroid was chosen to achieve a simple mechanical design and assembly: We preferred a single substrate that can be inserted into a package while requiring only one mechanical tolerance: the distance from the input to the output RF plane. We furthermore wanted to mount the transistor chip directly on a metal heatsink/ground while its top surface remaining at approximately the same height as top of the duroid and the electrical traces (to allow short bondwires). Hard-clad duroid was perfect for this type of arrangement as it provided all the requirements without the need for any additional mechanical tolerance. Milling out the dielectric in the center of the substrate and gold-plating it allowed a) placement of the HEMT chip directly onto the copper-backing and b) establishing good thermal and electrical contact to the substrate.

Fig. 7 Amplifier circuit diagram (Agilent ADS)

The amplifier design was performed using ADS [26]. Neither device models nor Process Design Kit were available for these HEMTs. To work around this, we based the design on small-signal and load/source pull measurements obtained on a previous run with same transistor design. The input match was realized as an *L*-match with an inductor formed by the gate terminal bond-wire plus the DC blocking capacitor parasitic inductance, and a shunt capacitor formed by open ended stubs. Wire-bonding was done using 1-mil gold wire. The real part of the output impedance was around 400 Ω. In order to create a λ/4 transformation from 50 Ω to 400 Ω needed to match the desired output matching impedance, one would need a 2-μm wide transmission line which is impractical. To avoid this, we first transform 50 Ω to ~20 Ω using an open ended stub parallel to 50 Ω and the parasitic series inductor of the DC blocking cap. We then use an 89 Ω, quarter-wavelength transmission line (125-μm width) to transform this to 400 Ω. The drain-terminal bond wire model is included in the output match. The amplifier circuit model is shown in Fig.

7, while the close-up on the mounted transistor is shown in Figure 8. The complete layout can be seen in the package in Figure 10.

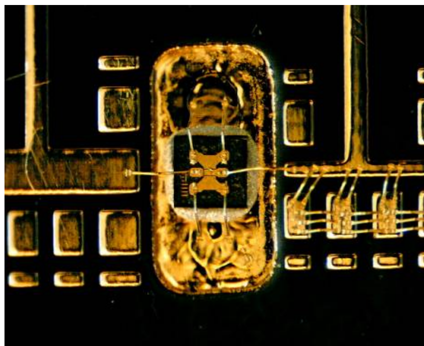

Fig. 8 – Close up image of the GaN-on-diamond HEMT with 200-μm gate periphery mounted in the amplifier shown in Fig. 8.

The bias circuit was designed to exhibit a parallel impedance of more than 1 kΩ over the frequency of interest and is included into the match. The stability was confirmed for the entire frequency range from 100 MHz to 15 GHz. The substrates also include tuning pads for fine adjustment. The expected peak output power was 800 mW CW.

The HEMT chip is attached to the substrate using H20 epoxy [27]. The ground pads (source contacts) were wire-bonded to the ground on the substrate with four bondwires. We applied wedge-bonding to all of our bonding in an attempt to minimize the bond-wire length. Figure 8 shows magnified images of the completed hybrid amplifiers. The mechanical format of our amplifier substrate (1.0" x 0.8") allows assembly for characterization by mounting coplanar end-launch connectors [28] to it (mechanical contact from the top; no soldering) and then attaching the substrate to an in-house designed 2" x 2" heatsink with fins that allow forced air cooling. This is practical for characterizing sample quantities of substrates as the connectors need to be mounted for each test. Over 20 amplifiers were assembled and tested.

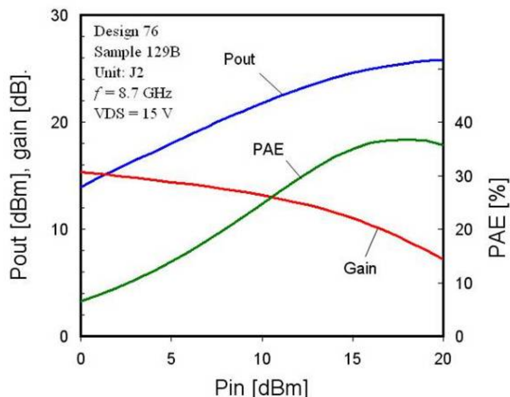

Fig. 9 Amplifier biased for highest output power

The performance of the amplifiers was optimal between 8.7 and 8.9 GHz with small-signal gain exceeding 16 dB and return loss better than −6 dB. Figure 9 shows typical small-signal measurements. The highest output power obtained was 380 mW with PAE > 35% at 15V supply voltage (see Figure 10). This output power is equivalent to 1.9 W/mm. Maximum PAE of 42% was recorded for a different amplifier. The deviation from the design frequency and expected peak power is primarily due to differences in the performance of the devices whose RF parameters were used to design the amplifier and the devices that were actually installed onto the amplifier substrates, namely, lower breakdown voltage limiting drain bias. The cause of this reduction is attributed to correctable process-related problems present on these two runs. Finally, we observed that the best amplifier modules performed better than best HEMTs measured on the wafer (1.9 W/mm versus 1.6 W/mm). We attribute this to better device heat sinking in the amplifier module.

V. PACKAGING

Taking advantage of diamond's high heat conductivity requires great care in packaging design. One of the essential difficulties in high-frequency packaging is realizing simultaneous high-frequency electrical contact to the RF lines and thermal contact between the die and the outside heatsink. Both of these contacts require mechanical pressure or soldering.

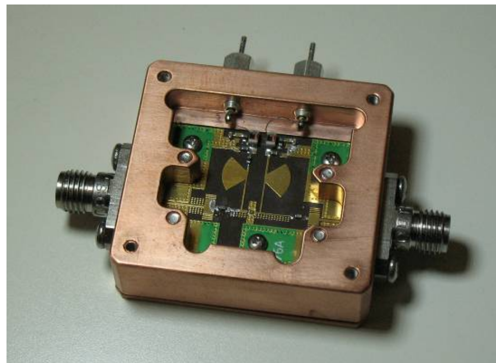

Fig. 10 Completed X-band amplifier module (lid removed)

We designed a high-thermal-conductance microwave package, shown in Fig. 10. The amplifier substrate (copper-clad duroid) fits into this package. This package has a unique assembly sequence illustrated in Fig. 11. It is common in the industry to make the heat-sinking surface a part of the package housing, but this approach requires precise (zero-tolerance) mechanical alignment between the electrical and thermal contact surfaces. In our approach, the heatsink and the package housing independently attach to the amplifier substrate and by doing so simultaneously offer: (i) pressurized mechanical/electrical contact between the package/connectors and the substrate transmission lines, and (ii) heat path from the die to the bottom surface of the package via direct pressurized mechanical contact. The coax-to-coplanar waveguide transition realized by pressure from the top of the substrate, is visible from Fig. 12. The center conductor may also be soldered to the coplanar traces. Completed amplifier modules feature SMA connectors [28] and DC filter-terminals for gate and drain bias. The dimensions of the package are 1.39" x 1.29" x 0.39"; the material is aluminum with copper bottom heatsink.

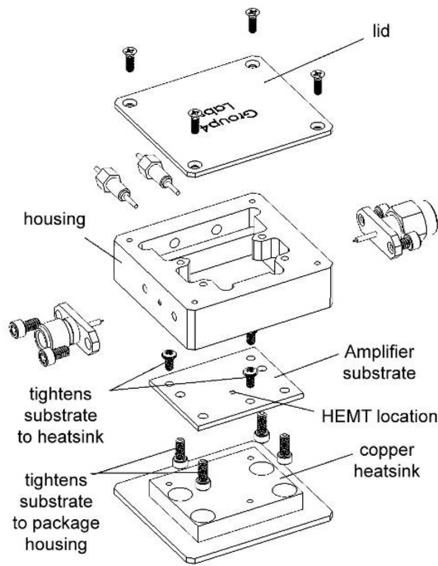

Fig. 11 – Amplifier module package

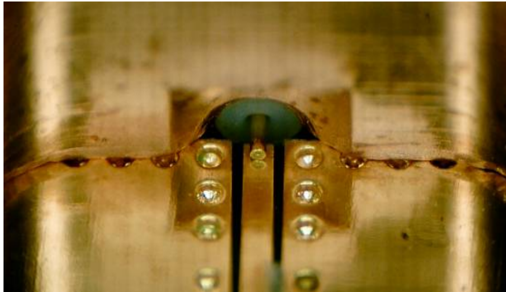

Fig. 12 Coax-to-coplanar waveguide transition in the package

VI. Thermal Resistance

The key aspect of diamond substrates is efficient heat spreading. To this end we measured the thermal resistance of the HEMTs mounted on the substrates using liquid crystal thermography. The test setup, schematically illustrated in Fig. 14, consistent of a stereo microscope with a polarized illuminator and a analyzer in the path of the light entering the microscope. The substrate with the HEMT die is placed on a hot-plate and a thermocouple is attached to the corner of the substrate for measuring its temperature. Only drain and source terminal were connected to a current source to deliver heating power. A variable power supply was used to deliver power to the HEMT; the dissipated power was measured using a voltmeter and an ammeter. A small quantity of nematic liquid crystal is then melted over the HEMT; the entire HEMT is immersed in the liquid crystal and the crystal phase-transitions to liquid at the melting temperature (in this case 104°C). We used a nematic-isotropic (N-I) transition at T_{LC} = 153°C (4-*n*-hexyloxybenzoic acid (CAS 1142-39-8) [29]. Polarized light is incident on the HEMT and the liquid crystal. The reflection is observed using a microscope through another polarizer (analyzer). The analyzer is adjusted to be 90° off from the polarization of the light incident on the HEMT. For temperatures below the N-I transition of the liquid crystal the reflection is bright. Once the temperature of any part of the HEMT reaches the N-I transition temperature those regions become dark, due to loss of polarization upon reflection. To make the measurement, we vary the hotplate temperature and for each setting we find the amount of power required to bring the center of the chip to reach the transition temperature. The electrical power is given by $P(T_{HS}) = (T_{LC}-T_{HS})/\Theta_{TH}$. From here, we set T_{HS}, then measure P and plot the data on a graph shown in Fig. 14. As the temperature of the heat sink increases it progressively takes less power to bring the top of the HEMT to the N-I transition temperature. The slope of the line gives the thermal resistance. The intercept on the horizontal axis is not equal the to N-I temperature because the absolute temperature reading is offset from the actual temperature below the chip. This offset is removed from the analysis by monitoring the relative change in power, i.e., the slope of the curve in Fig. 14. The measured thermal resistance was $\Theta_{TH} \approx$ 33°C/W.

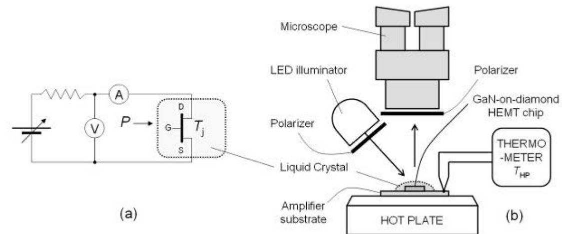

Fig. 13 – Liquid-crystal thermography setup

We also compared this result to the previously measured thermal resistance of GaN/SiC and GaN-on-diamond HEMTs using ThermoMicroscopes AFM-based SThM system on HEMTs with similar dimensions where GaN-on-diamond and GaN-on-SiC HEMTs exhibit $\Theta_{TH} \approx$ 30°C/W and $\Theta_{TH} \approx$ 60°C/W thermal resistance, respectively [16]. The comparison between the data obtained in this work and reference [16] is shown in Figure 15. The excellent match between these measurements confirms that diamond substrates indeed have an advantage over silicon carbide substrates by factor of two in thermal conductance.

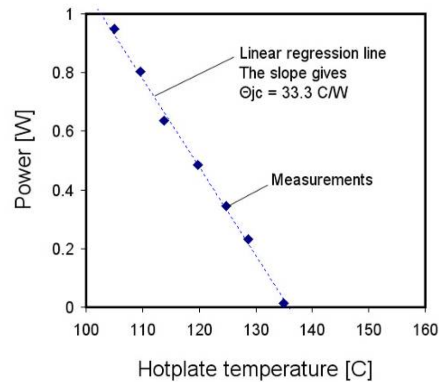

Fig. 14 – Power vs. heatsink temperature measurements

We also compared this measurement to theory using a 3D finite-difference thermal solver. We used assumed 10-μm thick epoxy with κ_{epoxy} = 0.29 W/cmK [27], and a 2.5-μm wide heat-source to get thermal resistance $\Theta_{TH} \approx$ 36°C/W which is <10% higher than the measured value possibly due to inaccurate thermal conductivity and thickness values. In addition, up to 5% of the power is being dissipated on the ohmic contacts that are spread out more than the source-to-

drain spacing. This theoretical analysis shows that the thermal resistance is dominated by the AlGaN/GaN layers rather than the diamond thermal conductivity, namely, more than 75% of the temperature rise occurs in the GaN/AlGaN, while the epoxy layer takes about %5. The thermal resistance of the GaN/AlGaN layers can be further reduced by etching off the nucleation layers prior to diamond attachment. In this way, the diamond can be brought to within 100's of nanometers to the heat producing area.

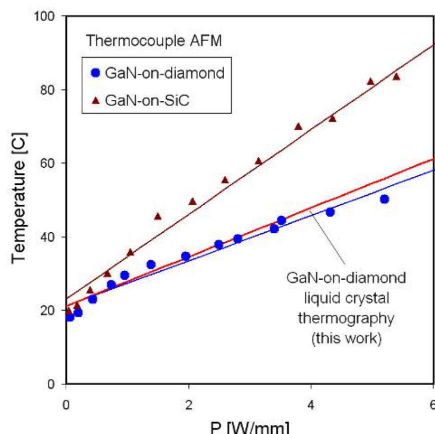

Fig. 15 Comparison between the thermal-resistance measurements using Liquid Crystal Thermography in this work with the measurements reported in reference [16].

VII. Conclusion

The essential elements of hybrid RF power amplifiers based on GaN-on-diamond technology have been demonstrated: GaN-on-diamond HEMTs have been built, wafers processed into devices, scribed and cleaved, and die mounted into packages. Thermal resistance measurements on the same amplifier substrates confirm that diamond heat-spreading and lower thermal-conductance packaging will give a designer of GaN-based high-power microwave components thermal management solutions that are superior to any other available technology on the market.

Acknowledgment

This work was supported in part by generous SBIR grants from MDA and AFRL (John Blevins). Other parts were also funded by SBIR grants from NASA (Lihua Li and Arnold Silva). Additionally, this work would not have been possible without the technical assistance provided by Dr. Earl McCune, Dr. Rick Compton, and Dr. Chandra Khandavalli.

References

[1] R. Quay, *Gallium Nitride Electronics*, Springer-Verlag Berlin Heidelberg (2008)

[2]. S. Nakamura, S. Chichibu (eds.), *Introduction to Nitride Semiconductor Blue Lasers and Light Emitting Diodes,* Taylor and Francis, London New York (2000).

[3] E. O. Johnson, "Physical Limitation on frequency and power parameters of transistors", *RCA Review*, p. 163-177, 1965.

[4] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications", *IEEE Electron Device Lett*., vol. 10, pp. 455, 1989.

[5] P.R. Hageman, J.J. Schermer, P.K. Larsen, *Thin Solid Films* 443 (2003) 9.

[6] P.W. May, H.Y. Tsai, W.N. Wang, J.A. Smith, *Diamond and Related Materials* 15 (2006) 526.

[7] M. Oba, T. Sugino, *Diamond Relat. Mat.* 10 (2001) 1343.

[8] J. W. Zimmer, "Enhancing Semiconductors with Diamond," *Mater. Res. Soc. Symp. Proc.* 956, p. 2007.

[9] E. Piner, J. W. Zimmer, J.C. Roberts, G. Chandler, R.A. Sadler, Extended Abstracts 33rd WOCSDICE, Málaga, Spain, p. 18, 2009.

[10] A. Dussaigne, M. Maliverni, D. Martin, A. Castiglia, N. Grandjean, „(0001) GaN grown on (111) single crystal diamond substrate for high power electronics applications", Proc. 18th European Workshop on Heterostructure Technology (HETECH 2009), 2-4 November 2009, Ulm, Germany, p. 33 (2009).

[11] D. Francis, F. Faili, D. Babić, F. Ejeckam, A. Nurmikko, H. Maris, "Formation and characterization of 4-inch GaN-on-diamond substrates", *Diam. Rel. Mat.,* online (2009).

[12] D. Francis, J. Wasserbauer, F. Faili, D. Babić, F. Ejeckam, W. Hong, P. Specht, and E. R. Weber, "GaN HEMT Epilayers on Diamond Substrates: Recent Progress," CS MANTECH, Austin, TX (May 14–17, 2007).

[13] Q. Diduck, J. Felbinger, L. F. Eastman, D. Francis, J. Wasserbauer, F. Faili, D. I. Babić, F. Ejeckam, "Frequency performance enhancement of AlGaN/GaN HEMTs on diamond", *Electron. Lett.* vol. 45, p. 758, 2009.

[14] J. G. Felbinger, L. F. Eastman, J. Wasserbauer, F. Faili, D. I. Babić, D. Francis, F. Ejeckam, "AlGaN/GaN-on-Diamond HEMT Recent Progress", WOCSDICE 2009, Málaga, Spain, May 17-20, session Mon4, pp. 22-24, 2009.

[15] K. D. Chabak, J. K. Gillespie, V. Miller, A. Crespo, J. Roussos, M. Trejo, D. E. Walker, Jr., G. D. Via, G. H. Jessen, J. Wasserbauer, F. Faili, D. I. Babić, D. Francis, F. Ejeckam, "Full-wafer characterization of AlGaN/GaN HEMTs on free-standing CVD diamond substrates", *IEEE Electron. Dev. Lett*., vol. 31, no. 2, pp. 99-101, 2010.

[16] J.G. Felbinger, et al., "Comparison of GaN HEMTs on Diamond and SiC Substrates," *IEEE Electron Device Letters*, vol. 28, no. 11, p. 948 (2007)..

[17] To be published.

[18] Nitronex Corporation, NC, USA (www.nitronex.com)

[19] J. E. Graebner, S. Jin, G. W. Kammlott, J. A. Herb, C. F. Cardinier, "Unusually high thermal conductivity in diamond films", *Appl. Phys. Lett*. vol. 60, pp. 1576-1578, 1992.

[20] Medium-tack dicing tape, www.semicorp.com, p/n 18551-7.50.

[21] N. B. Dahotre, and S. P Harimkar, *Laser Fabrication and Machining of Materials*, Springer Science + Business Media, 2008.

[22] V. V. Kononenko, T. V. Kononenko, S. M. Pimenov, M. N. Sinyavkii, V. I. Konov, F. Dausinger, "Effect of the pulse duration on graphitization of diamond during ablation", *Quantum Electronics* 35 (2005) 252-256.

[23] T. V. Kononenko, V. G. Ralchenko, I. I. Vlasov, S. V. Garnov, V. I. Konov, "Ablation of CVD diamond with nanosecond laser pulses of UV-IR range", *Diam. Rel. Mat.* 7 (1998) 1623-1627.

[24] Laserod, Inc., Torrance, CA; (www.laserod.com).

[25] Rogers Corporation, CT, www.rogerscorp.com.

[26] Agilent Technologies, Santa Clara, CA, USA.

[27] Epotek Technology, Inc., Massachusetts, USA.

[28] Southwest Microwave, Inc. Tempe, Arizona, USA.

[29] Alfa Aesar, Massachusetts, USA (www.alfa.com)