

**GROUP4LABS**  
AN EXTREME MATERIALS COMPANY

**Pioneering Devices Through Materials Innovations**

# **A 2D model of the temperature profile of discrete heat-generating chips on a diamond substrate**

**(A companion document to the January 21<sup>st</sup> 2006 document)**

Prepared for designers of HEMTs, FETs, lasers, LEDs, and thermal-intensive semiconductor devices

March 29<sup>th</sup>, 2006

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# INTRODUCTION

Group4 Labs' GaN-on-Diamond technology enables the placement of GaN heat sources (embedded in GaN epilayers) within sub-nanometer proximity to highly thermally conductive CVD diamond substrates. The calculations presented here show that this proximity can lead to a 10X to 100X or more increase in the power density of an array of heat-producing electronic/photonic devices. In some operating conditions, GaN-on-Diamond devices operate where GaN-on-traditional substrates falter.

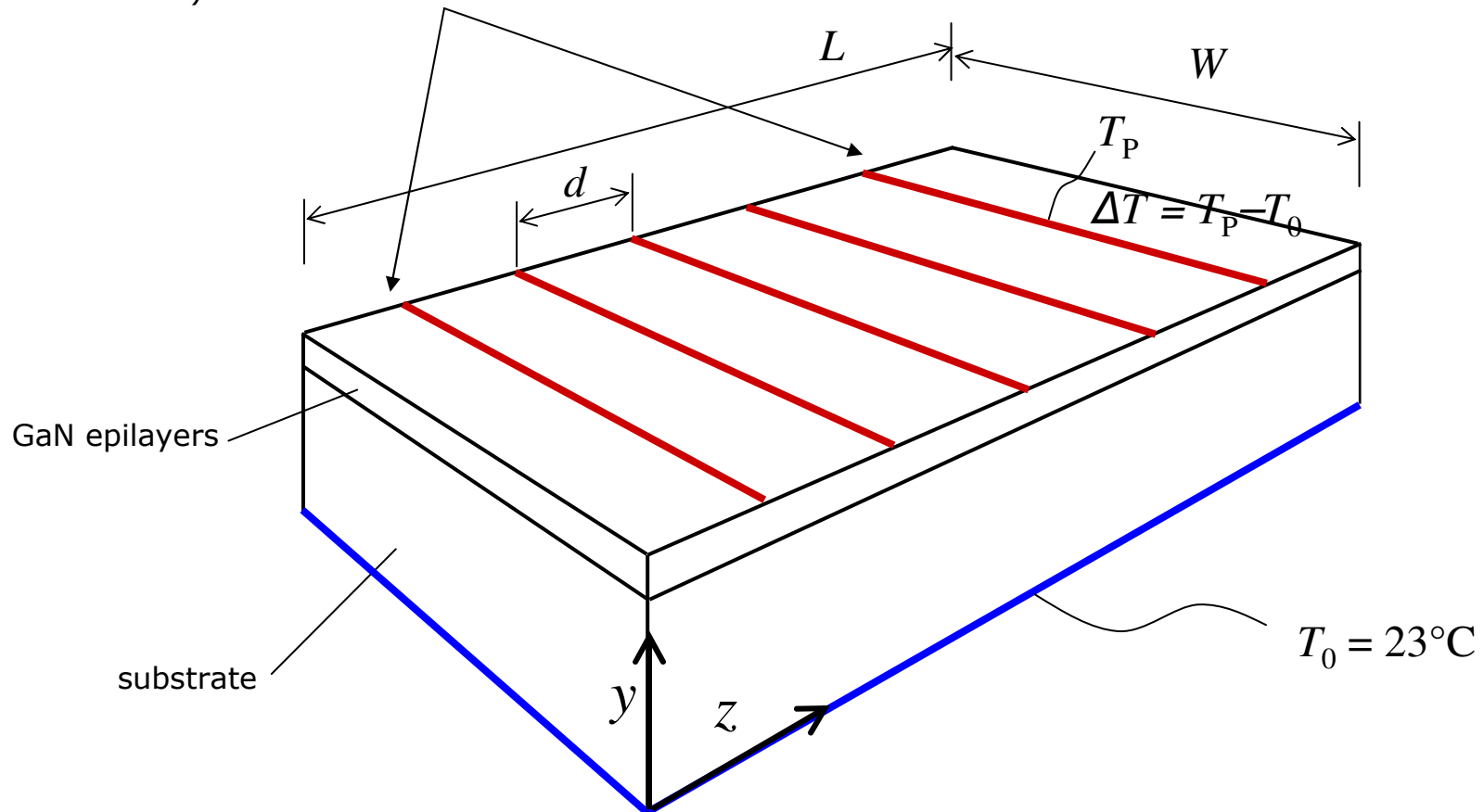
The power output capacity (power per unit area) of a high-electron-mobility-transistor (HEMT), field-effect-transistor (FET), or other such device is limited by its highest operating temperature. The transistor gate's operating temperature is determined by its linear power dissipation, expressed in W/cm, the spatial separation between the gates, and the thermal conductivity of the material structure below the gate. Note that the gates of modern high-power HEMTs are generally formed in a linear array of heat sources; thus, the smallest possible separation between the sources is limited by the highest allowed operating temperature of each source.

Chemically-vapor-deposited (CVD) diamond possesses a higher thermal conductivity (1200 W/m/K) than the conventional substrates used for epitaxial GaN growth: sapphire (40 W/m/K), silicon (149 W/m/K), and silicon carbide (350 W/m/K). The purpose of this presentation is to simulate/model how the use of CVD diamond in place of conventional GaN substrates might dramatically improve the performance of an heat-producing device such as a HEMT or FET. The results presented here allow the device designer to place gates (i.e. linear heat sources) significantly closer together when CVD diamond is used as a substrate – so that the total power density per chip is amplified.

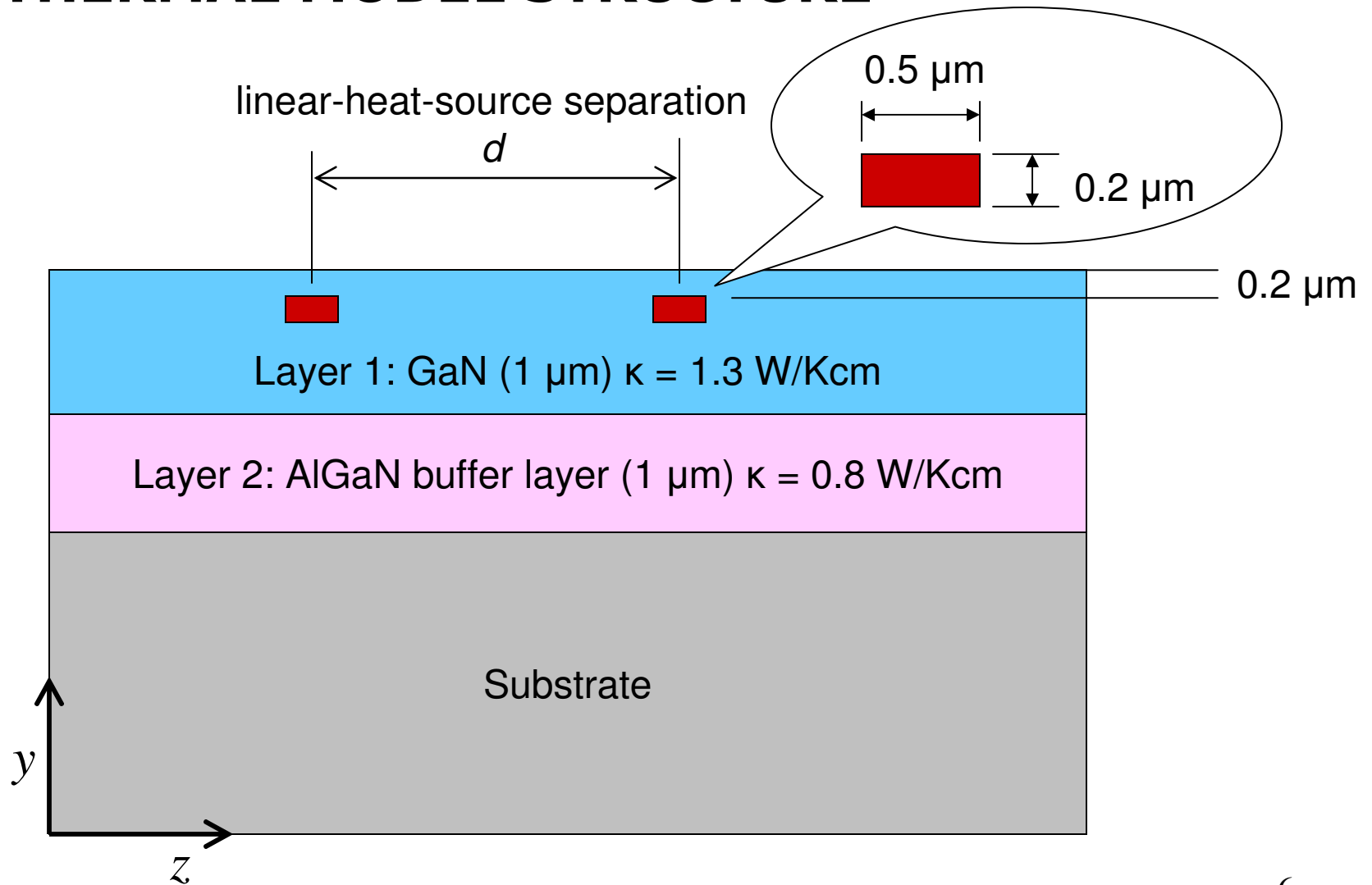
In the particular case of GaN epitaxy, it should be noted that Group4 Labs' technology allows the placement of GaN epi-layers directly onto a CVD diamond without the traditional buffer or nucleation layers typically used in the conventional growth of GaN. Such buffer/nucleation layers harbor poor thermal conductivity that adversely impacts the gate operating temperature and thus overall performance.

# THERMAL MODEL STRUCTURE

Array of linear heat-generating devices on GaN  
(length of heat sources is long in comparison with the separation  $d$  and width of the sources)



# THERMAL MODEL STRUCTURE



## DEVICE STRUCTURE ASSUMPTIONS

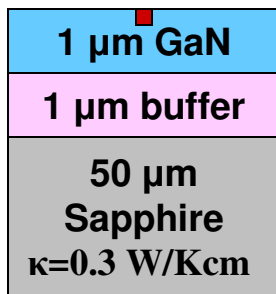
- Length of each chip ( $L$ ): 3mm
- Gate length ( $W$ ): 150-microns
- Carrier beneath the substrates is assumed to be an infinite and perfect thermal conductor
- Chip Power Density presented here is defined as Watts per Area ( $L*W$ ) given a device's (active junction) maximum allowable operating temperature

# MATERIALS PROPERTIES

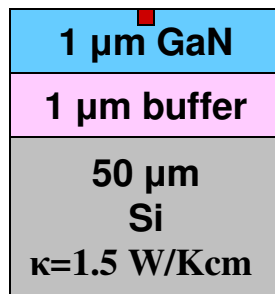
<b>Materials</b>	<b>Thermal Conductivity [W/K/cm]</b>
Si	1.49
GaAs	0.46
GaN	1.30
AlGaN Buffer average	0.80
Cu	4.01
SiO <sub>2</sub>	0.03
SiC	3.50
CVD Diamond	10.0
SiN	0.3
Sapphire	0.4

# SUBSTRATE THICKNESS CASE #1

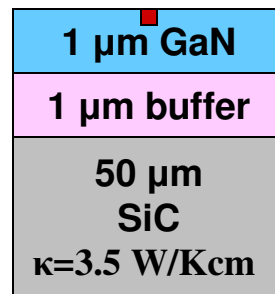
(a)



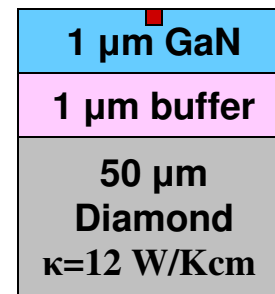
(b)



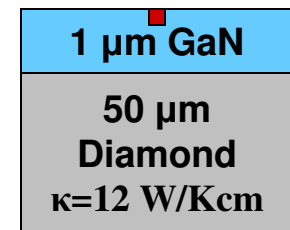
(c)



(d)

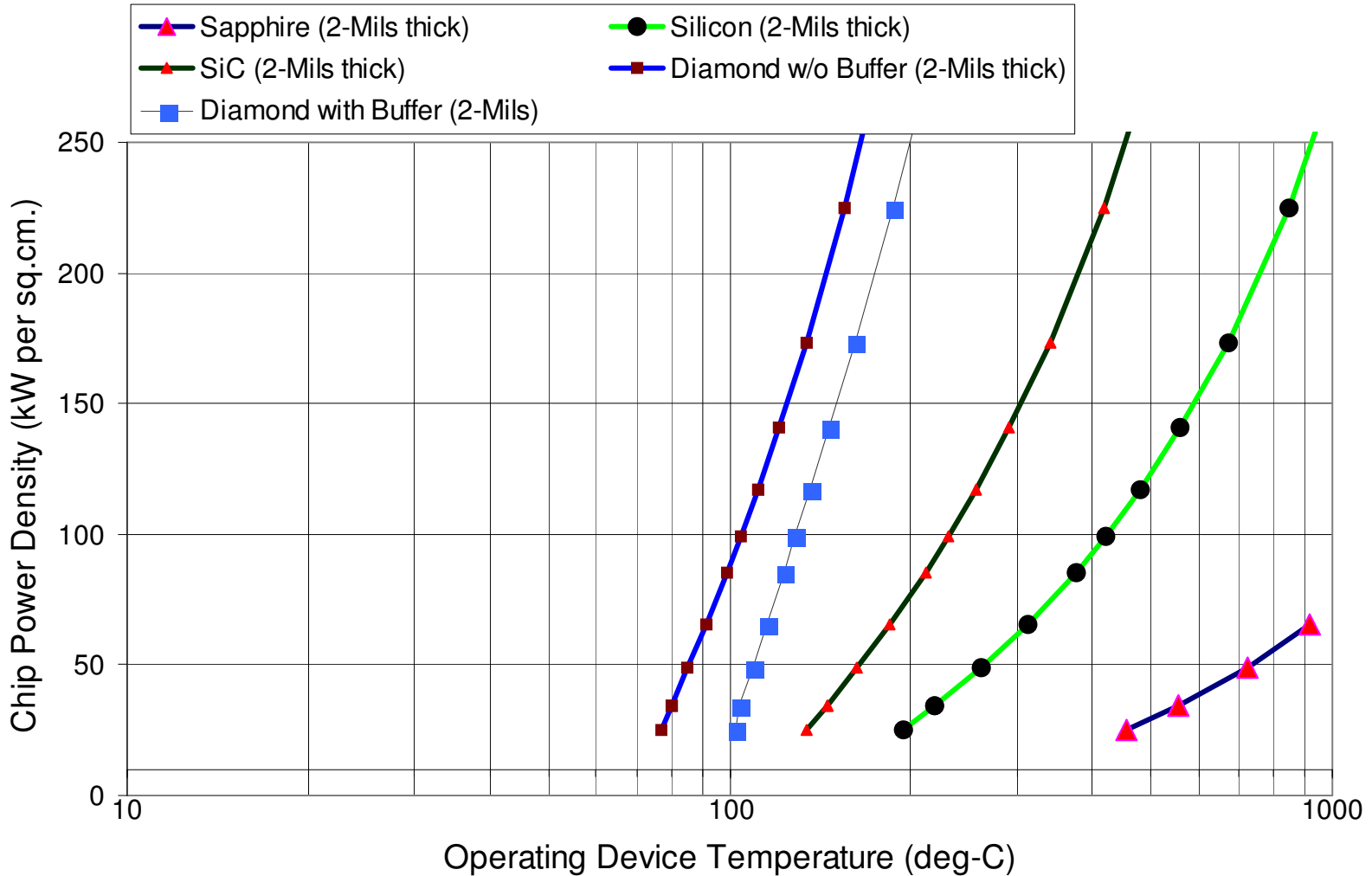


(e)



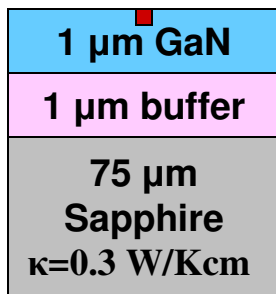
Transistor packing density assumes a gate input power at 100 W/cm

# SUBSTRATE THICKNESS CASE #1

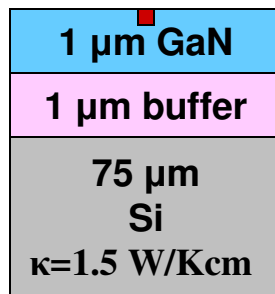


## SUBSTRATE THICKNESS CASE #2

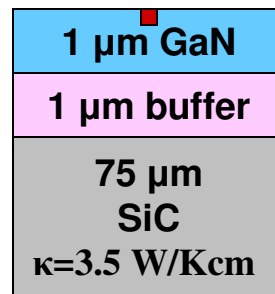
(a)



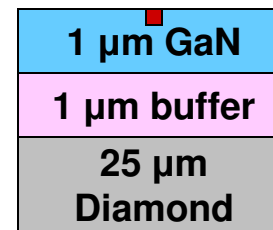
(b)



(c)



(d)

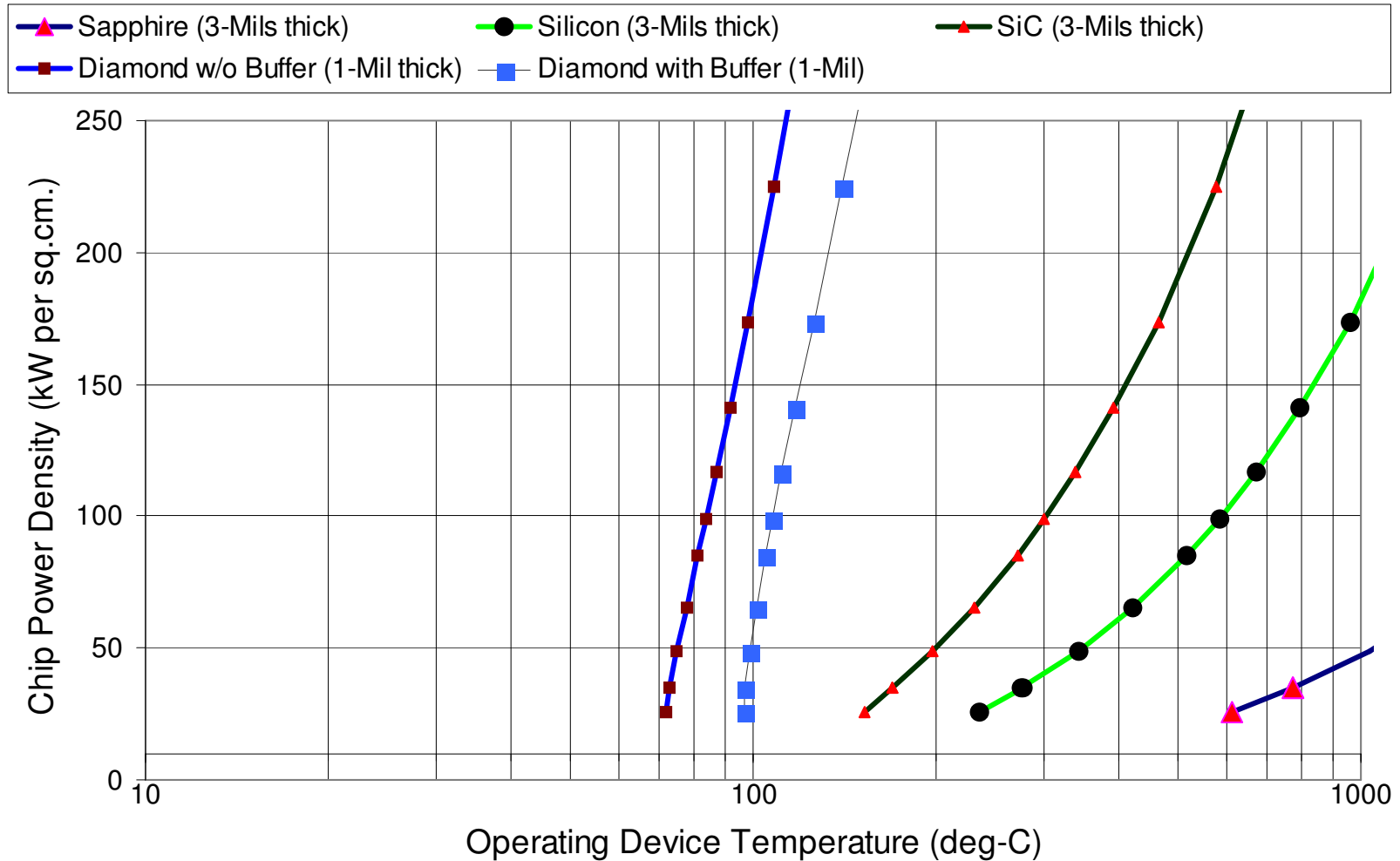


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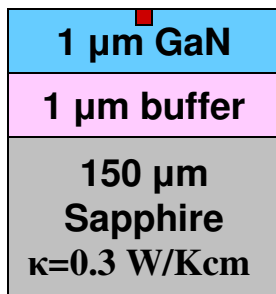
Transistor packing density assumes a gate input power at 100 W/cm

## SUBSTRATE THICKNESS CASE #2

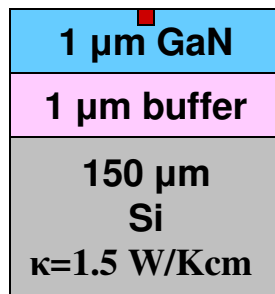


## SUBSTRATE THICKNESS CASE #3

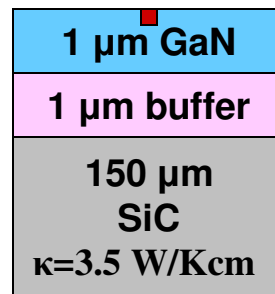
(a)



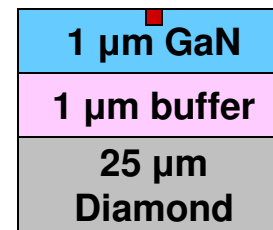
(b)



(c)



(d)



(e)



Transistor packing density assumes a gate input power at 100 W/cm

# SUBSTRATE THICKNESS CASE #3

