

GROUP4LABS
AN EXTREME MATERIALS COMPANY

Pioneering Devices Through Materials Innovations

A 2D model of the temperature profile of discrete heat-generating chips on a diamond substrate

Prepared for designers of HEMTs, FETs, lasers, LEDs, and other thermal-intensive semiconductor devices

January 21, 2006

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INTRODUCTION

Group4 Labs' GaN-on-Diamond technology enables the placement of GaN heat sources (embedded in GaN epilayers) within sub-nanometer proximity to highly thermally-conductive CVD diamond substrates. The calculations presented here show that this proximity can lead to a 20X or more increase in the power density of an array of heat-producing electronic/photonic devices. In some operating conditions, GaN-on-Diamond devices operate where GaN on traditional substrates

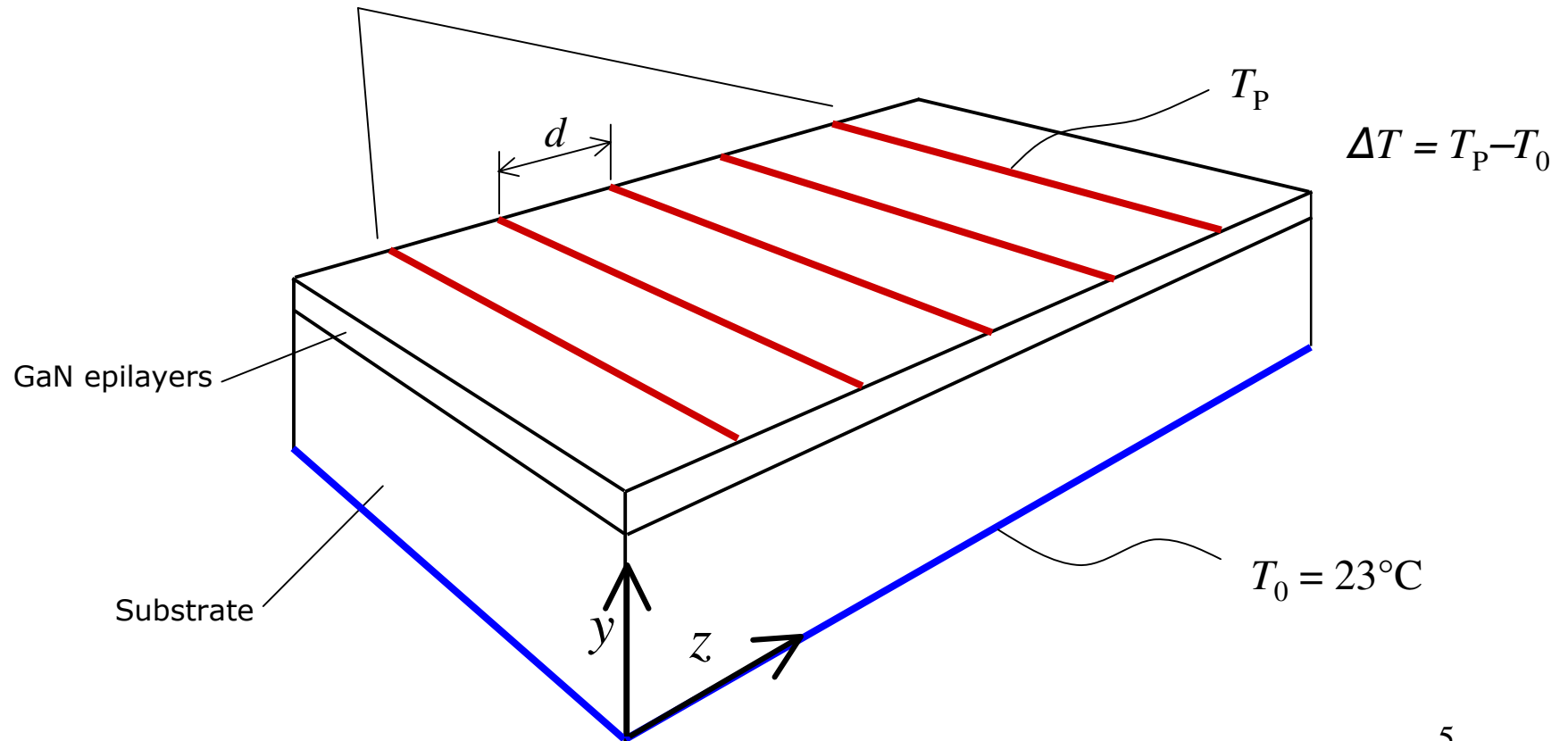
The power output capacity (power per unit area) of a high-electron-mobility-transistors (HEMTs), field-effect-transistors (FETs), or other such device is limited by its highest operating temperature. The transistor gate's operating temperature is determined by its linear power dissipation, expressed in W/cm, the spatial separation between the gates, and the thermal conductivity of the material structure below the gate. Note that the gates of modern high-power HEMTs are generally formed in a linear array of heat sources; thus, the smallest possible separation between the sources is limited by the highest allowed operating temperature of each source.

Chemically-vapor-deposited (CVD) diamond possesses a higher thermal conductivity (1200 W/m/K) than the conventional substrates used for epitaxial GaN growth: sapphire (40 W/m/K), silicon (149 W/m/K), and silicon carbide (350 W/m/K). The purpose of this presentation is to simulate/model how the use of CVD diamond in place of conventional GaN substrates might dramatically improve the performance of an heat-producing device such as a HEMT or FET. The results presented here allow the device designer to place gates (i.e. linear heat sources) significantly closer together when CVD diamond is used as a substrate – so that the total power density per chip is amplified.

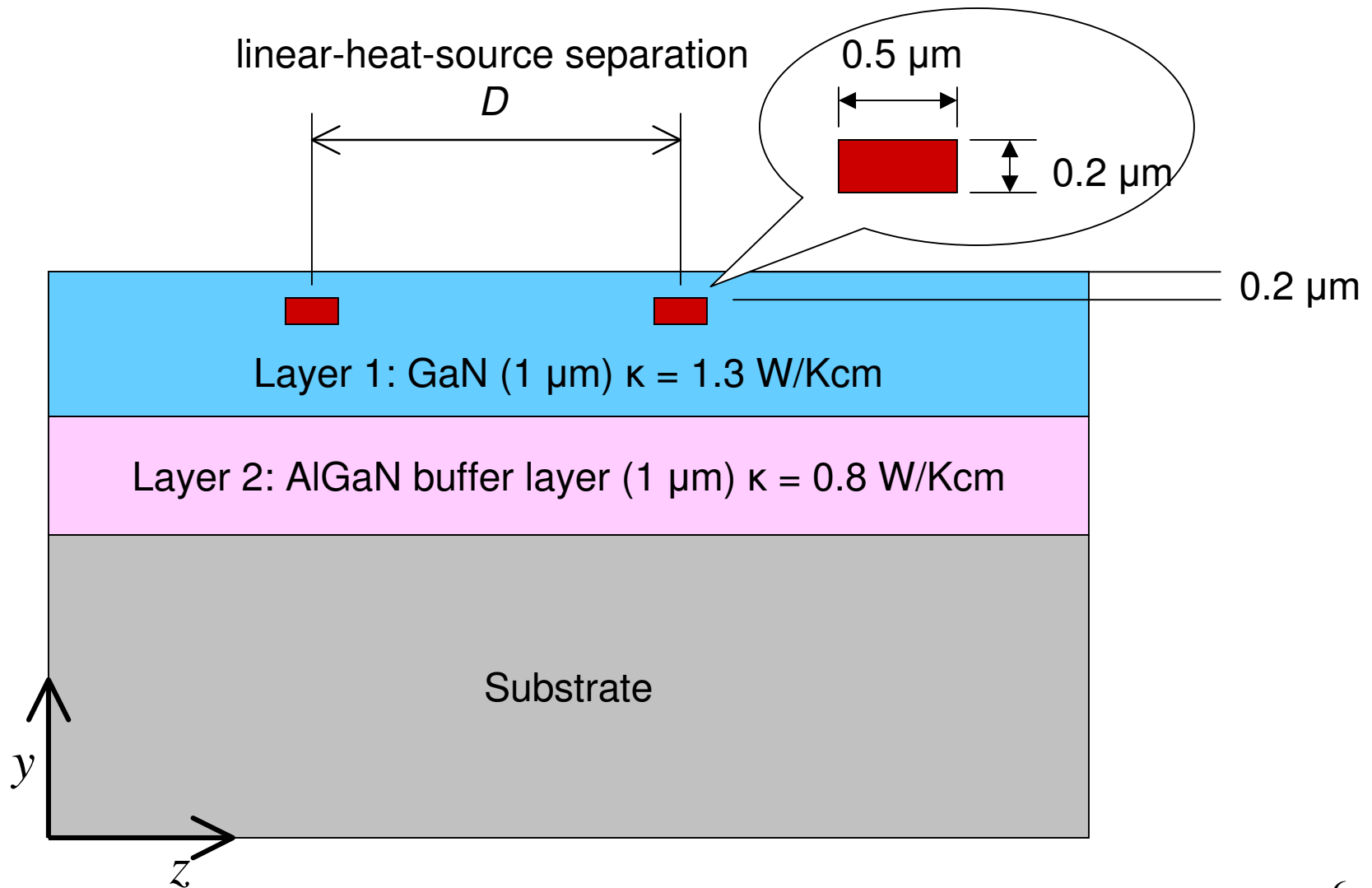
In the particular case of GaN epitaxy, it should be noted that Group4 Labs' technology allows the placement of GaN epi-layers directly onto a CVD diamond without the traditional buffer or nucleation layers typically used in the conventional growth of GaN. Such buffer/nucleation layers harbor poor thermal conductivity that adversely impacts the gate operating temperature and thus overall performance.

THERMAL MODEL STRUCTURE

Array of linear heat-generating devices on GaN
(length of heat sources is long in comparison with the separation d and width of the sources)

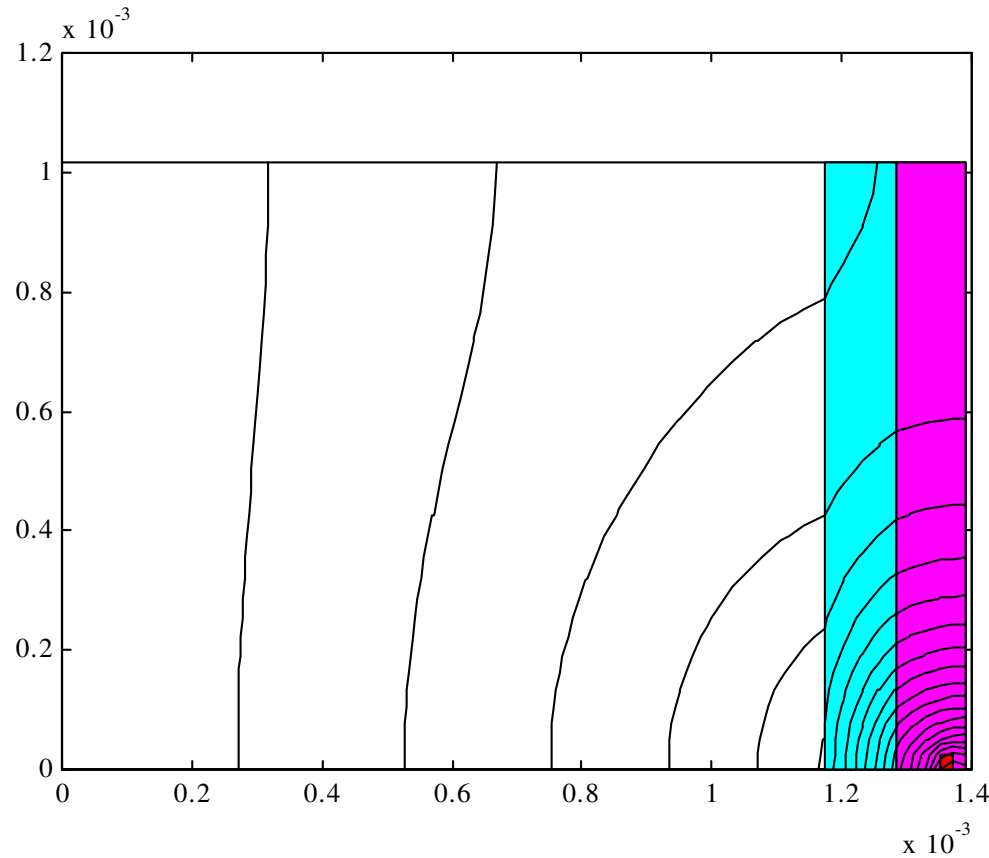


THERMAL MODEL STRUCTURE



Example of equal temperature curves

The heat flow calculations uses a two-dimensional finite difference method with a non-uniform mesh. The smallest mesh increments in y and z directions are $0.2 \mu\text{m}$ and $0.25 \mu\text{m}$, respectively.



MATERIALS PROPERTIES ASSUMPTIONS

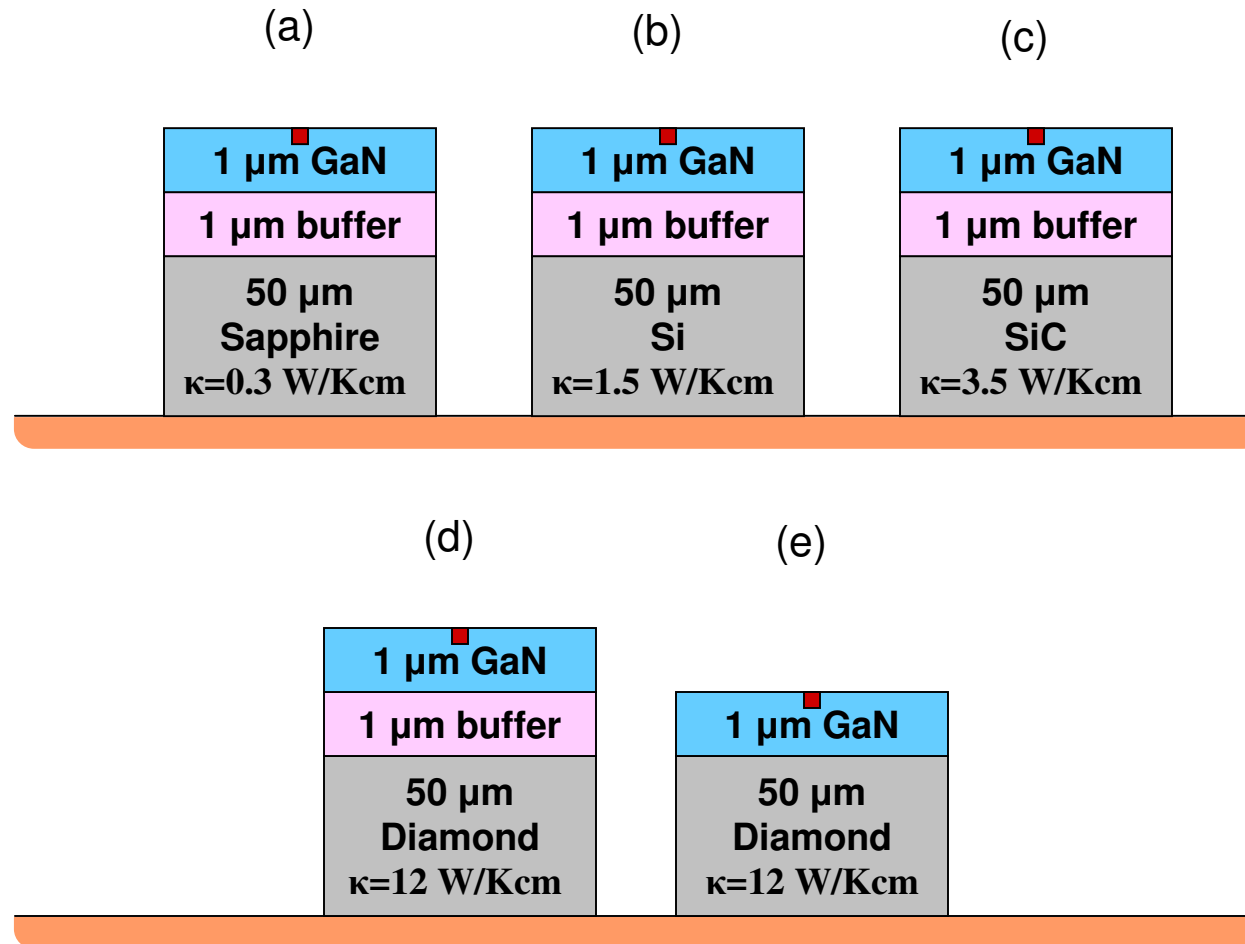
Materials	Thermal Conductivity [W/K/cm]
Si	1.49
GaAs	0.46
GaN	1.30
AlGaN Buffer average	0.80
Cu	4.01
SiO ₂	0.03
SiC	3.50
CVD Diamond (C)	10.0
SiN	0.3
Sapphire	0.4

SUMMARY OF CASES MODELED

There are three (3) cases modeled here, with each case comprising five (5) scenarios:

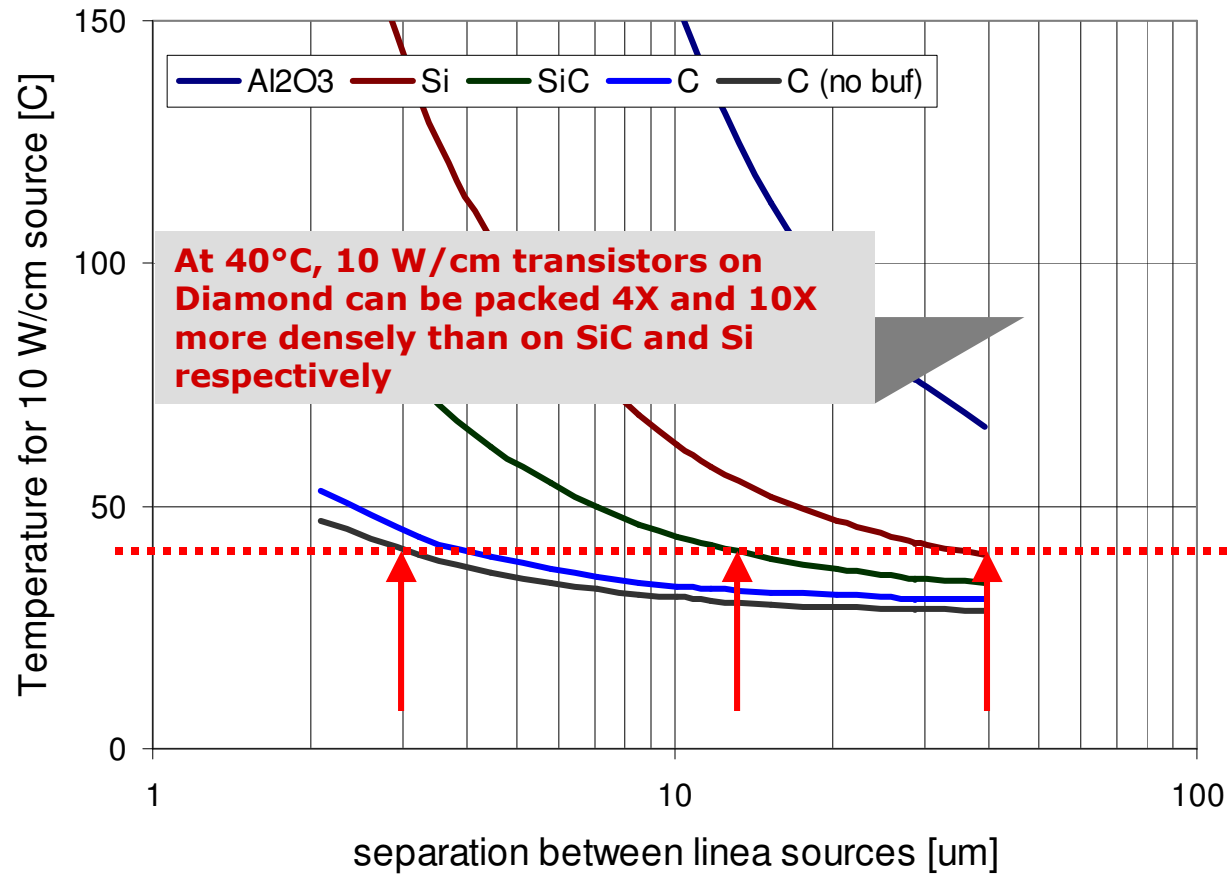
- Cases 1 thru 3 represent varying substrate thicknesses that have been chosen for their popular use in the GaN industry. Five scenarios (described below) of structures have been modeled for each of the three cases.
- Scenarios (a), (b), and (c) represent industry-standard GaN structures that can be grown directly on sapphire (Al_2O_3), silicon (Si), and silicon carbide (SiC) substrates respectively.
- Scenarios (d) and (e) represent structures possible with Group4 Labs technology – wherein gallium nitride (GaN) epilayers are atomically attached to CVD diamond; scenario (d) includes diamond with an AlGaN buffer/nucleation layer and scenario (e) includes no buffer/nucleation layer. Group4 Labs technology enables the removal of any buffer layer.
- All structures rest on a heatsink which is assumed to be at room temperature. The heat flow from the substrates into the heatsink is assumed uniform so that additional increases in temperature due to solders and copper heatsink thickness can be accounted in a straightforward manner.

SUBSTRATE THICKNESS CASE #1



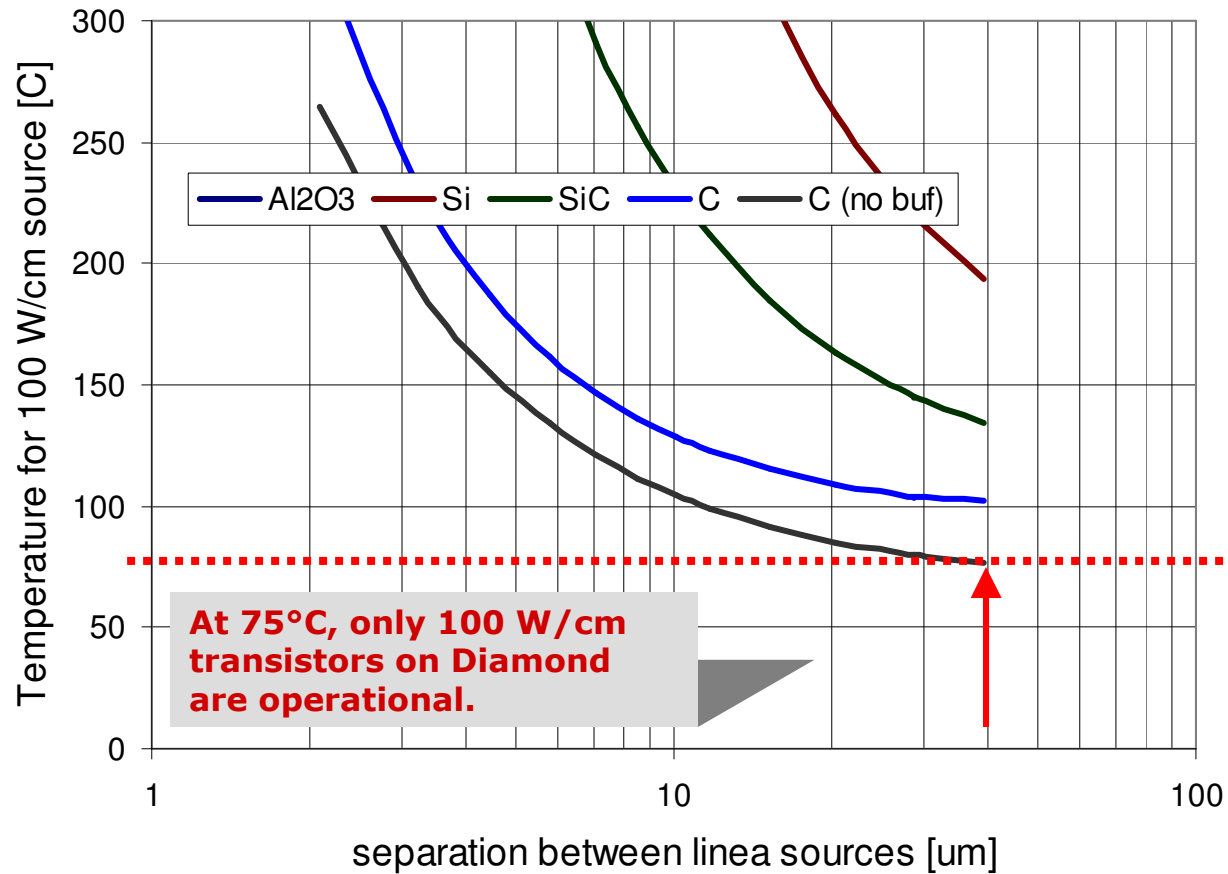
SUBSTRATE THICKNESS CASE #1

Peak (absolute) temperature assuming transistor's gate power at 10 W/cm, and the substrate's bottom at 23°C



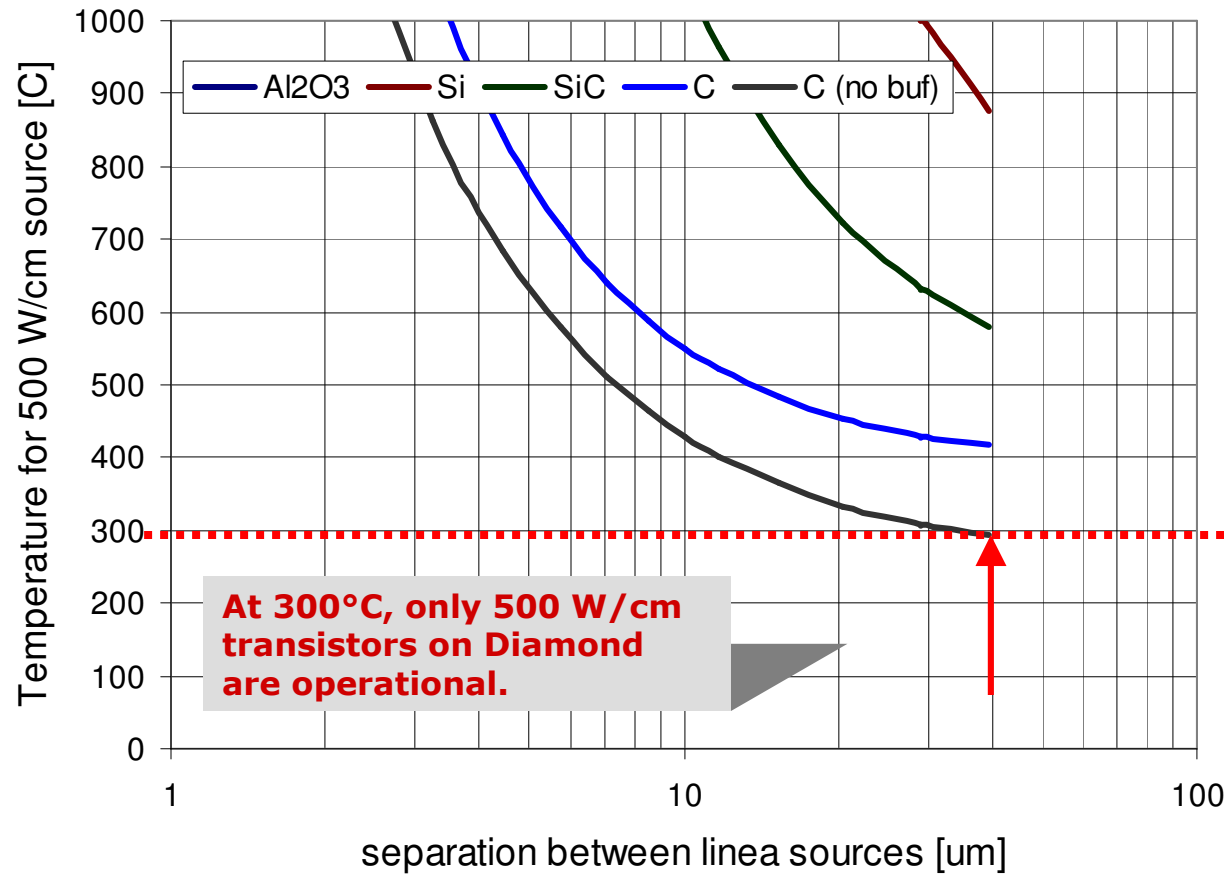
SUBSTRATE THICKNESS CASE #1

Peak (absolute) temperature assuming transistor's gate power at 100W/cm, and the substrate's bottom at 23°C



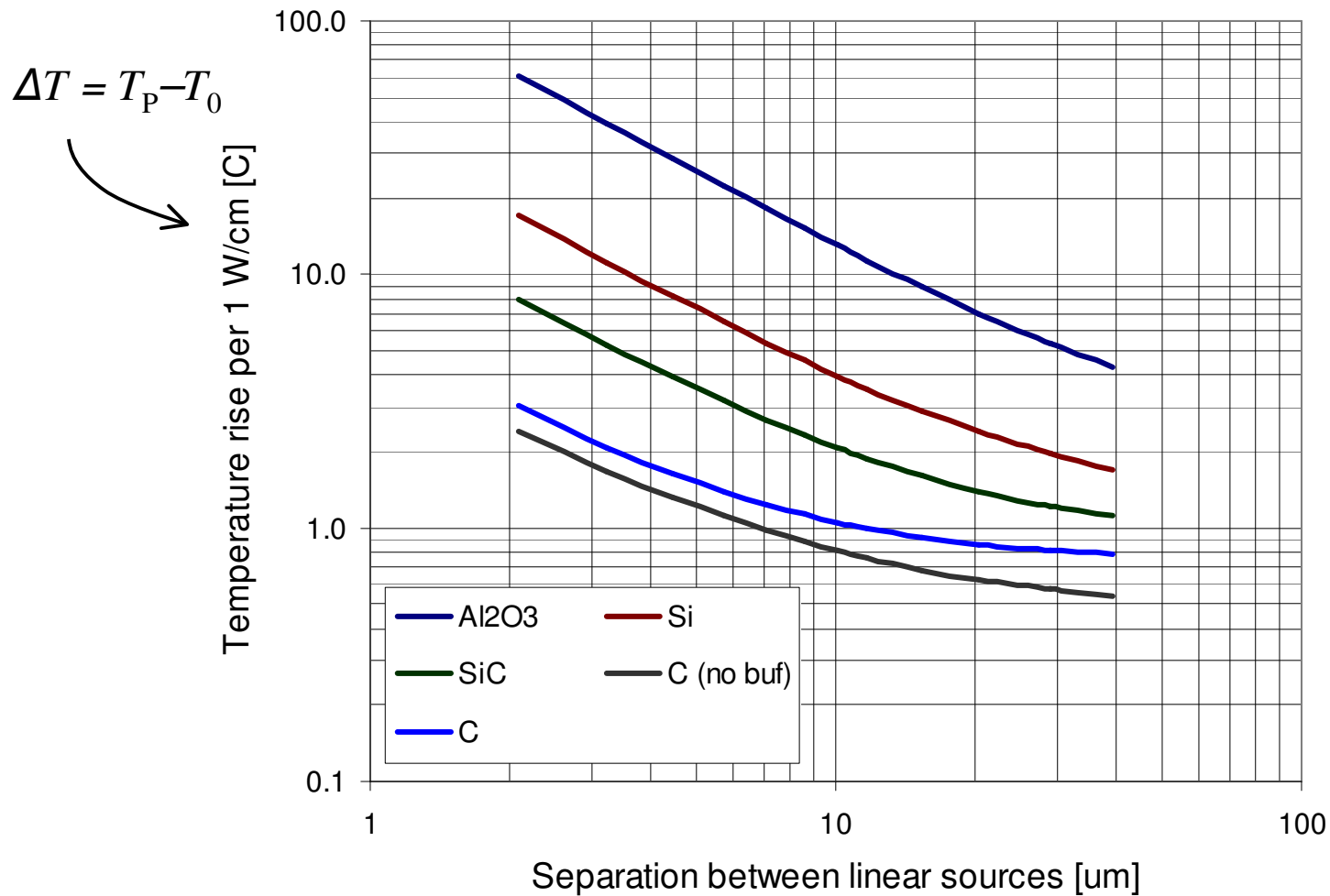
SUBSTRATE THICKNESS CASE #1

Peak (absolute) temperature assuming transistor's gate power at 500 W/cm and the substrate bottom at 23°C



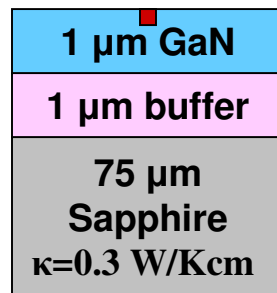
SUBSTRATE THICKNESS CASE #1

**Temperature rise relative to substrate's bottom
for each 1 W/cm in heat dissipation along the linear source (gate)**

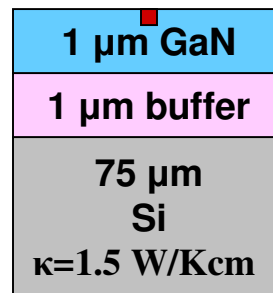


SUBSTRATE THICKNESS CASE #2

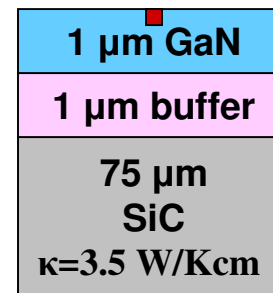
(a)



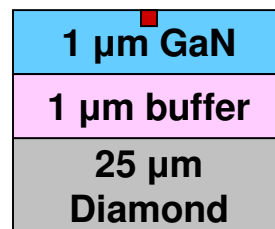
(b)



(c)



(d)

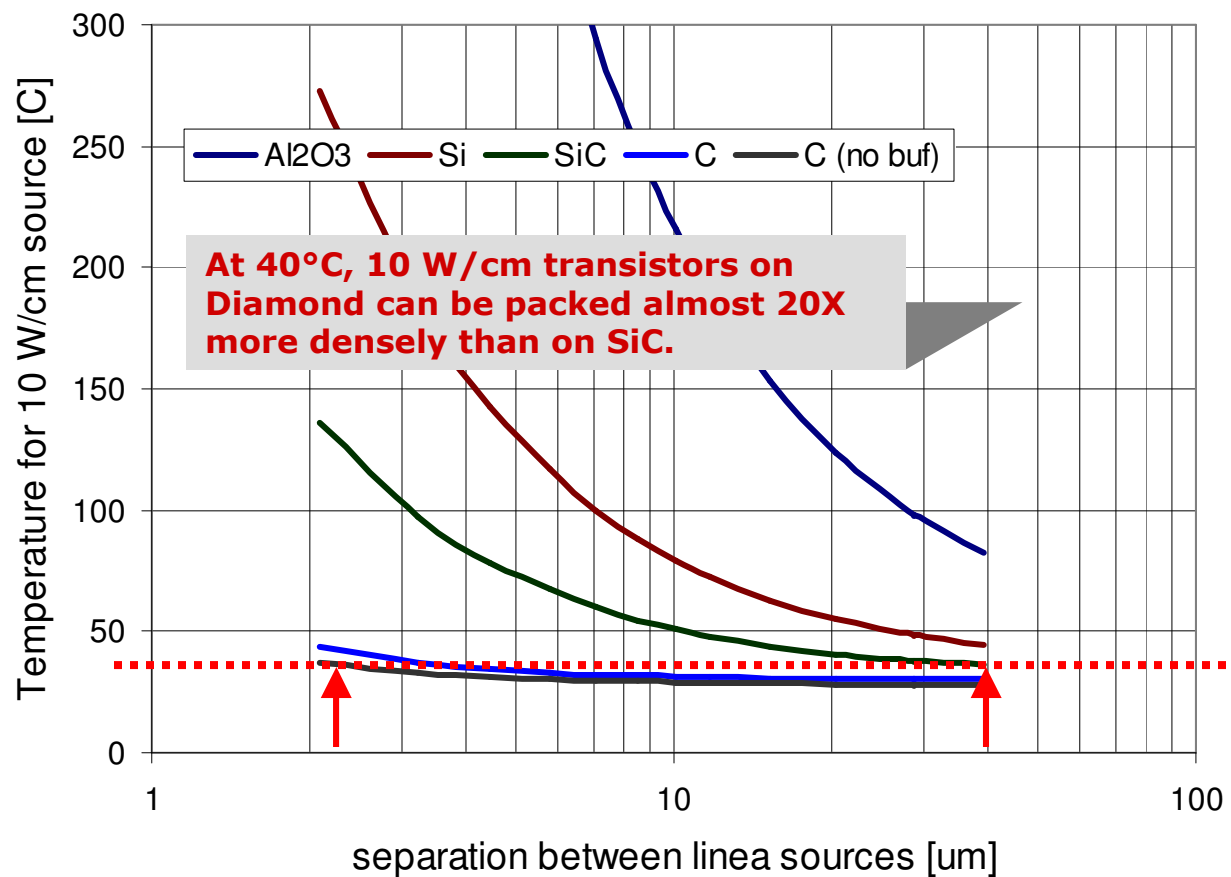


(e)



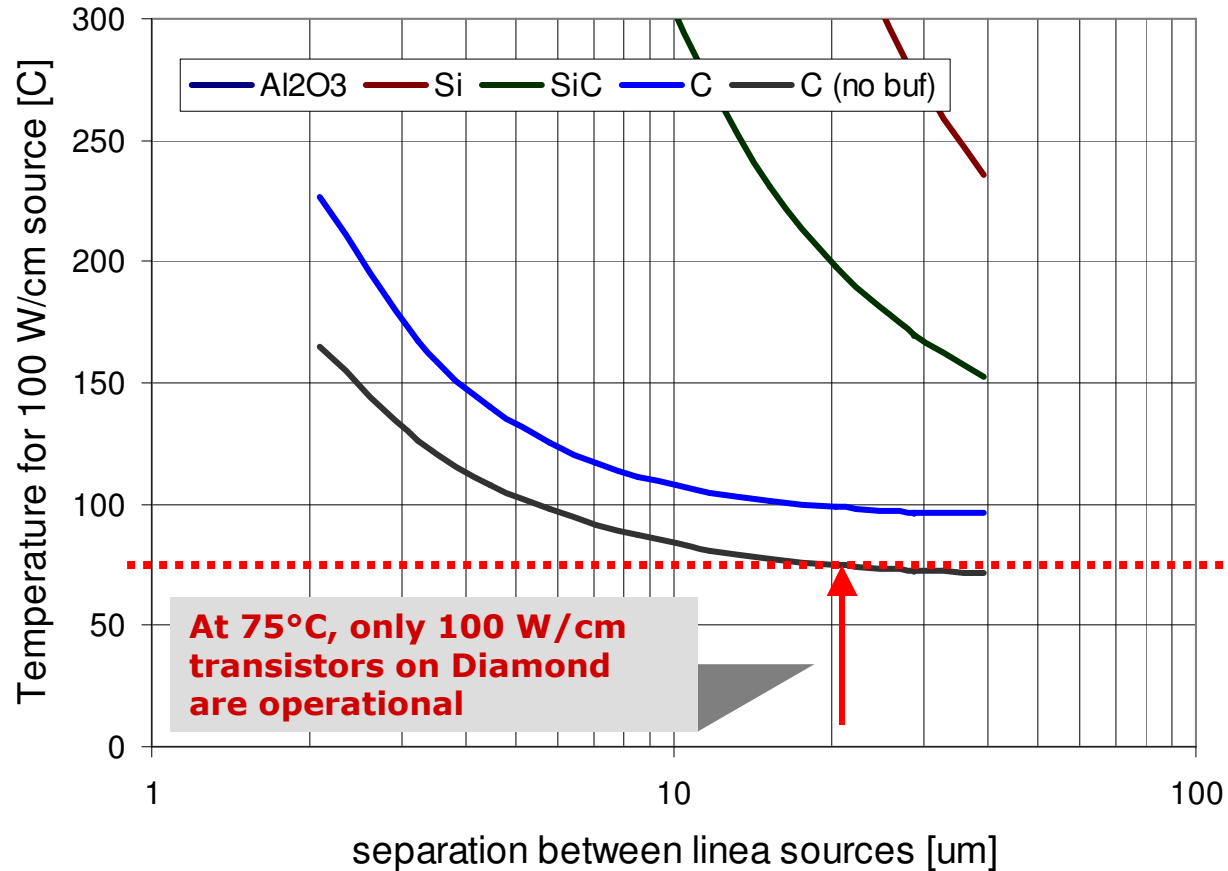
SUBSTRATE THICKNESS CASE #2

Peak (absolute) temperature assuming transistor's gate power at 10 W/cm, and the substrate's bottom at 23°C



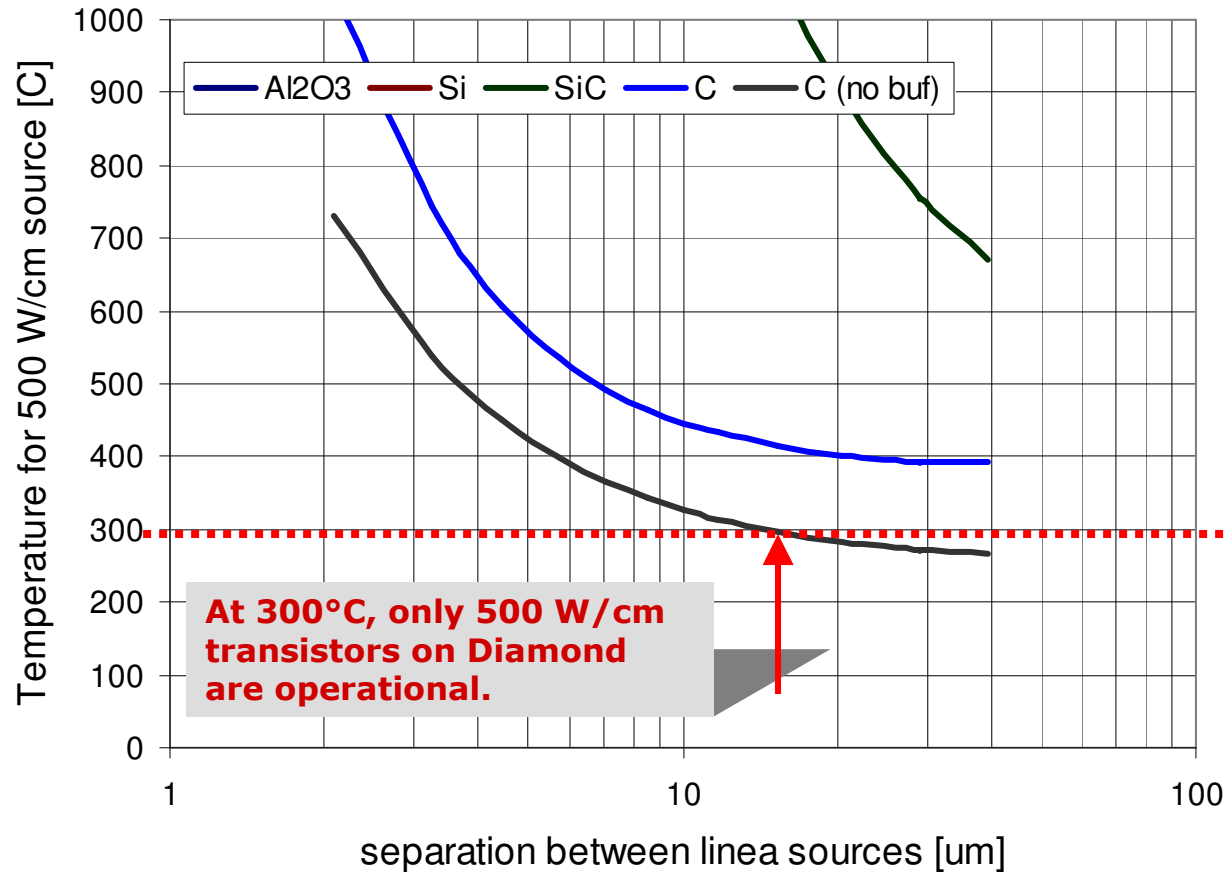
SUBSTRATE THICKNESS CASE #2

Peak (absolute) temperature assuming transistor's gate power at 100W/cm, and the substrate's bottom at 23°C



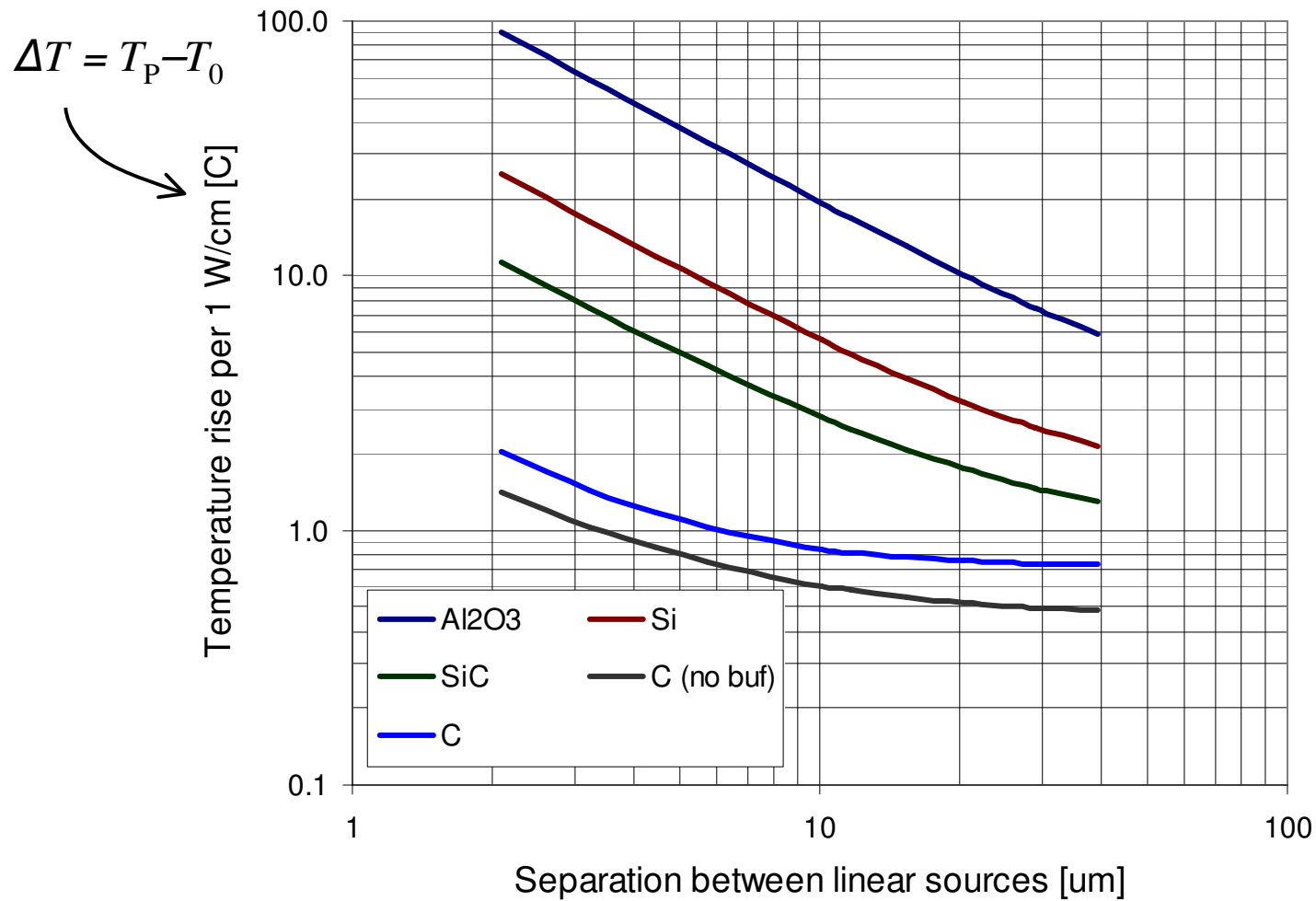
SUBSTRATE THICKNESS CASE #2

Peak (absolute) temperature assuming transistor's gate power at 500 W/cm and the substrate's bottom at 23°C



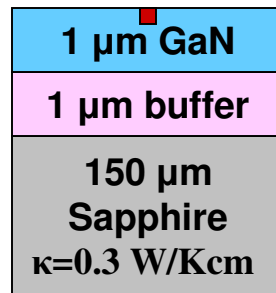
SUBSTRATE THICKNESS CASE #2

**Temperature rise relative to substrate's bottom
for each 1 W/cm in heat dissipation along the linear source (gate)**

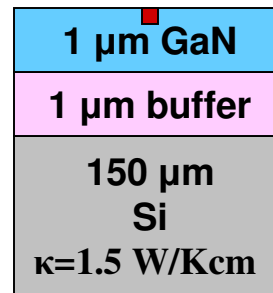


SUBSTRATE THICKNESS CASE #3

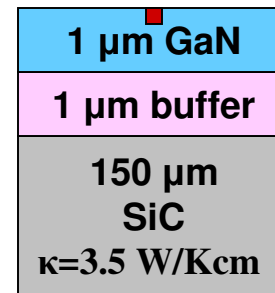
(a)



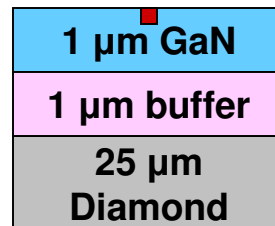
(b)



(c)



(d)

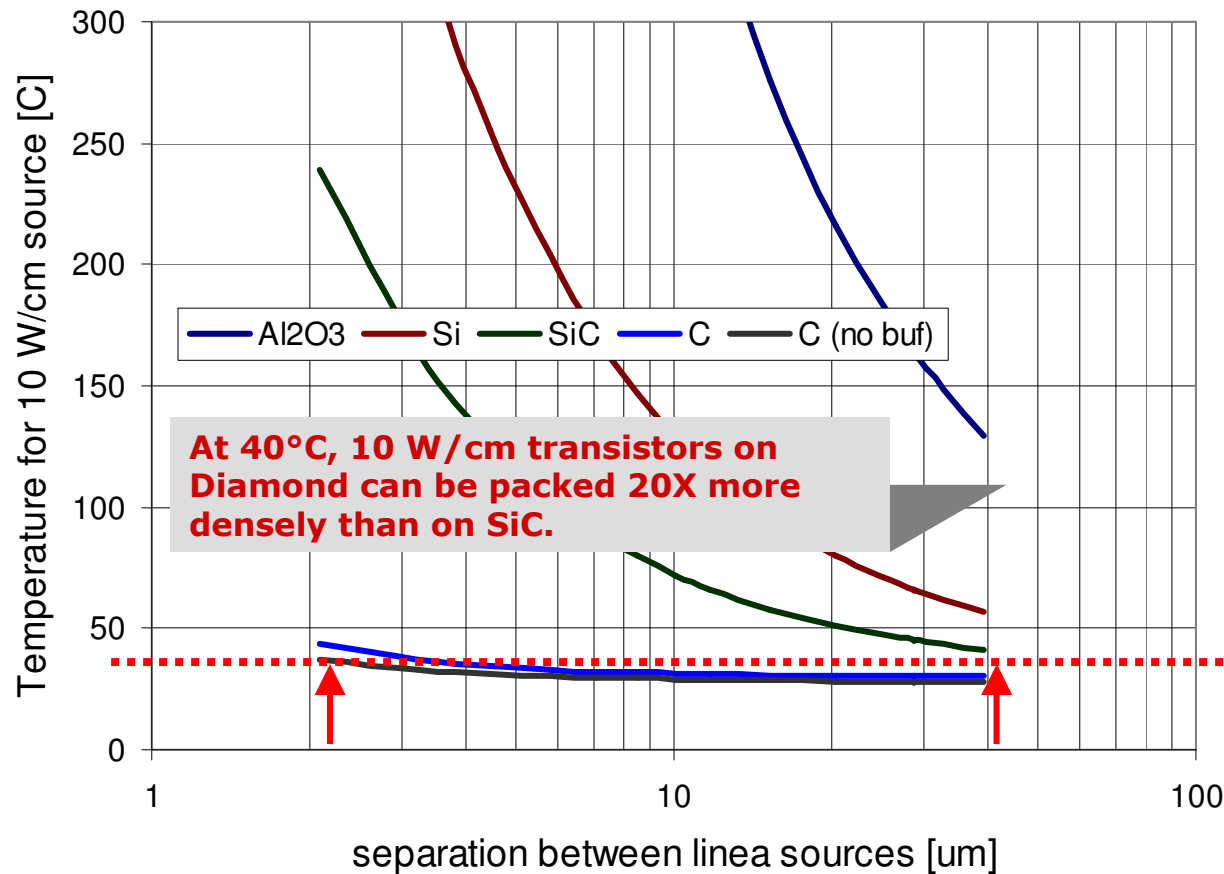


(e)



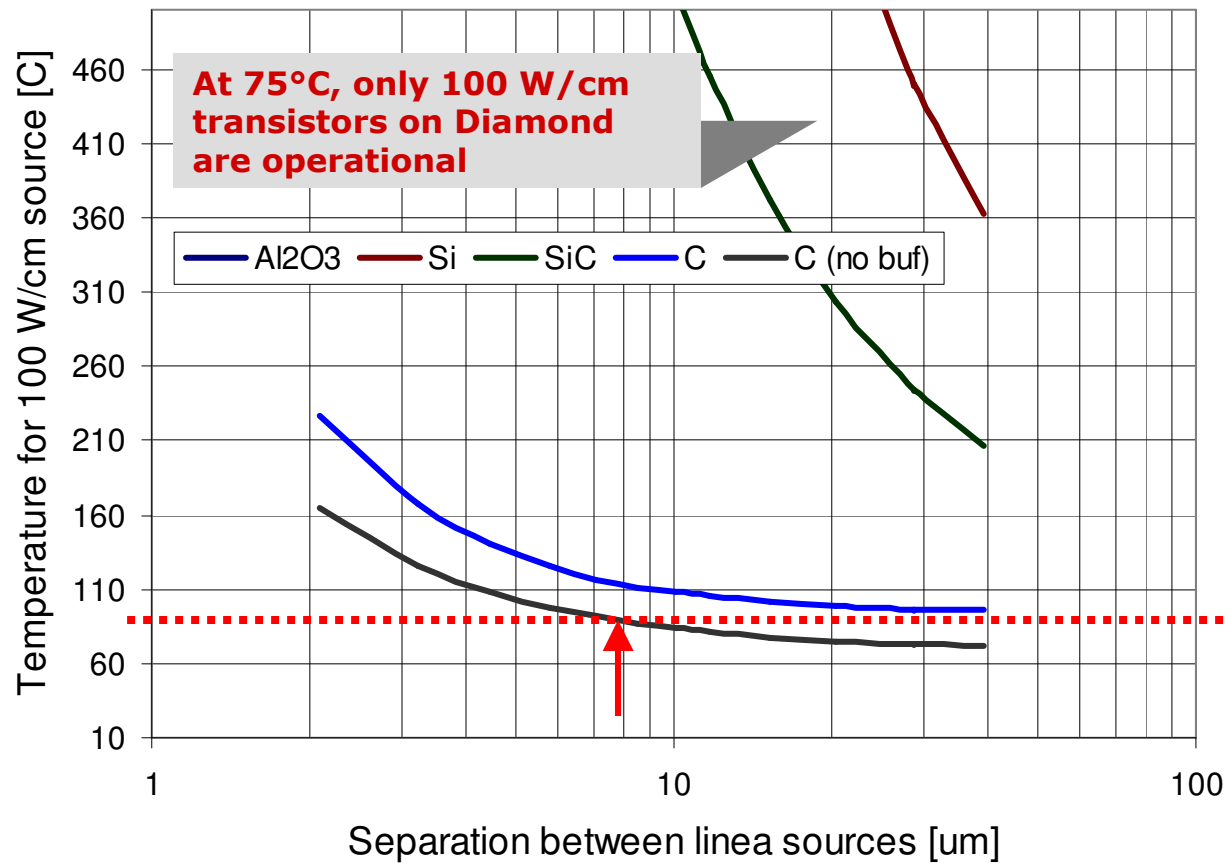
SUBSTRATE THICKNESS CASE #3

Peak (absolute) temperature assuming transistor's gate power at 10 W/cm, and the substrate's bottom at 23°C



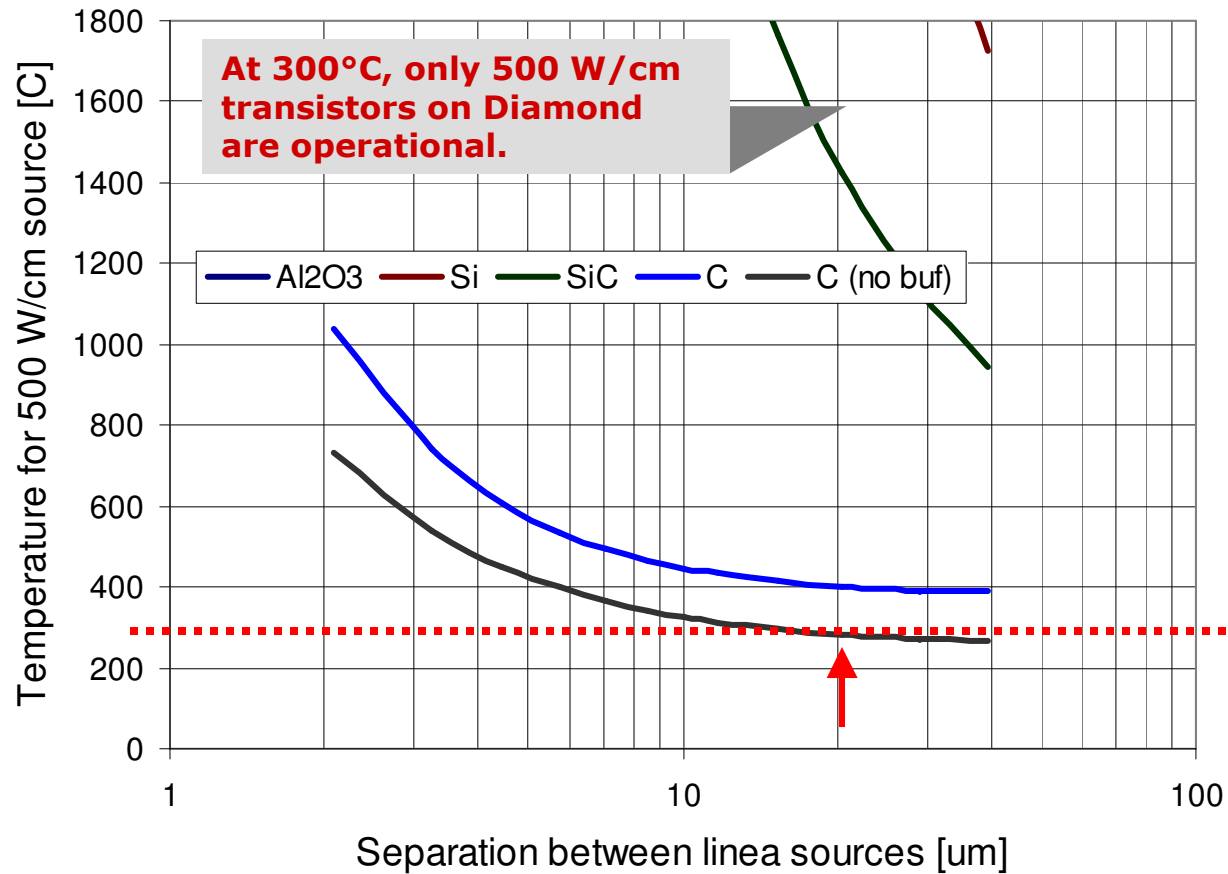
SUBSTRATE THICKNESS CASE #3

Peak (absolute) temperature assuming transistor's gate power at 100W/cm, and the substrate's bottom at 23°C



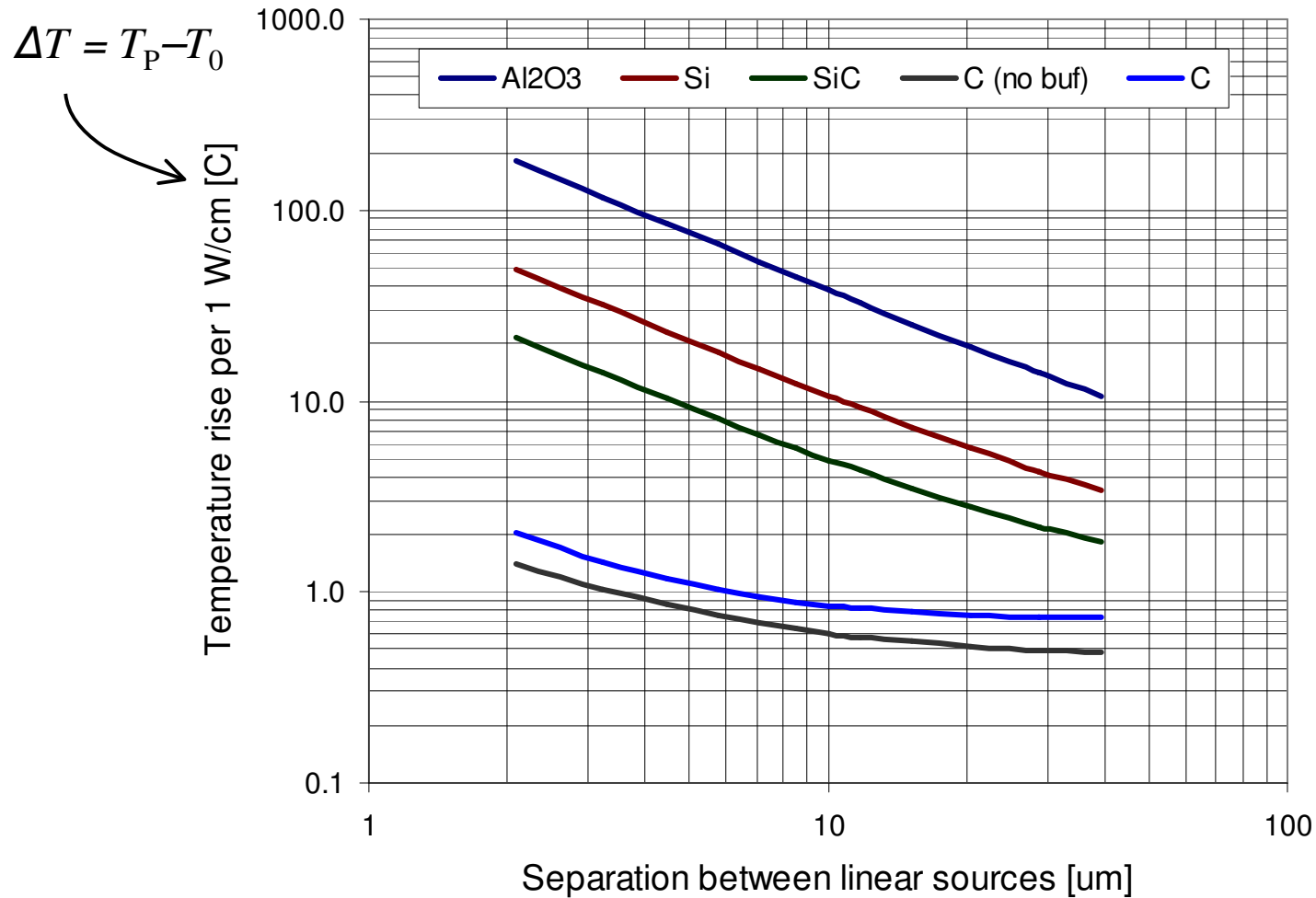
SUBSTRATE THICKNESS CASE #3

Peak (absolute) temperature assuming transistor's gate power at 500 W/cm and the substrate's bottom at 23°C



SUBSTRATE THICKNESS CASE #3

**Temperature rise relative to substrate's bottom
for each 1 W/cm in heat dissipation along the linear source (gate)**



RESULTS SUMMARY

Extent of power density improvement in a GaN-on-Diamond transistor compared to GaN-on-SiC transistors

	Case #1	Case #2	Case #3
10 W/cm devices at 40C	4X increase	20X increase	20X increase
100 W/cm devices at 75C	GaN-on-Diamond is operational; GaN-on-SiC is non-operational	GaN-on-Diamond is operational; GaN-on-SiC is non-operational	GaN-on-Diamond is operational; GaN-on-SiC is non-operational
500 W/cm devices at 300C	GaN-on-Diamond is operational; GaN-on-SiC is non-operational	GaN-on-Diamond is operational; GaN-on-SiC is non-operational	GaN-on-Diamond is operational; GaN-on-SiC is non-operational