

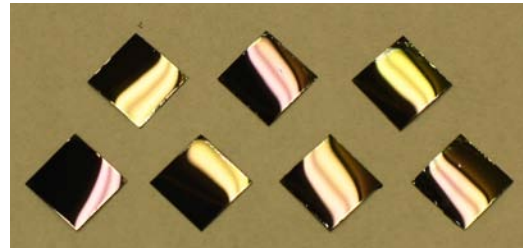
From the **Xero wafer family**

Template of a Gallium Nitride epitaxial layer on a diamond substrate

Nitrogen-terminated GaN-Surface
10mm x 10mm Wafers

PRODUCT FEATURES

- Epi-ready surface of epitaxial Gallium Nitride (GaN) on diamond substrate
- N-terminated $(0,0,0,\bar{1})$ Wurzite GaN
- Excellent thermal properties
- Very low dielectric loss
- Available as free standing 10mm x 10mm wafer or mounted on Silicon carrier substrate.



APPLICATIONS

- Epitaxial re-growth by MOCVD or MBE
- High-power and high-frequency GaN High Electron Mobility Transistors (HEMTs) and Field Effect Transistors (FETs)
- High-temperature environments
- High-power, high-temperature, and high-efficiency blue/green/white Light Emitting Diodes (LEDs)
- High-power and High-temperature UV/blue/green Lasers Diodes (LDs)

PRODUCT DESCRIPTION

What is it?

A Group4 Labs' Xero wafer is a 10-mm x 10-mm composite wafer featuring one epitaxial GaN layer atomically attached to a free-standing, 25-micron thick polycrystalline CVD diamond substrate. The GaN exposes a Nitrogen-terminated surface. The Xero wafer is immediately ready for epitaxial crystal growth. The wafer has been resilience tested up to 1200°C. The Xero wafer is available free standing (Option F) or mounted on a silicon wafer (Option H).

Why GaN-on-Diamond?

GaN and its alloys have the widest electronic bandgap and the highest breakdown voltage of any commercial semiconductor available today. To maximize the performance of GaN, chemical vapor deposition (CVD) diamond offers the largest thermal conductivity, second only to pure single-crystal diamond. A composite of GaN-on-Diamond material (where the GaN is fractions of a nanometer away from the diamond) will enable development of the most powerful transistors, LEDs, and lasers possible and will allow devices to operate at extremely high temperatures.

Group4 Labs' unique wafer-level integration technology opens doors to unprecedented freedom in extreme thermal design, and enables dramatic increases in the output power and overall performance of electronic and optical devices. Applications include high frequency and high-power HEMTs and MODFETs, high-temperature UV and blue/green laser diodes, and ultra-high brightness LEDs.

How we make it?

Group4 Labs uses a proprietary physio-chemical process to atomically attach high quality epitaxial GaN materials, grown by metal-organic CVD (MOCVD) to a CVD diamond substrate. There are no metals or organics embedded in the composite Xero wafer. The GaN layer rests about 0.5nm away from the diamond substrate.

RELATED ARTICLES

(Available online at www.Group4Labs.com/technology)

1. Simulations & Modeling of devices on GaN-on-Diamond
2. Fundamental properties of various GaN and Diamond related materials
3. How to process a GaN-on-Diamond wafers
4. Thermal cycling of GaN-on-Diamond wafers

TECHNICAL SPECIFICATIONS

	Min	Typical	Max	Units	Notes
GaN template layer properties					
Wafer dimension	9.8x9.8	10x10	10.1x10.1	mm ²	Fig. 3
Thickness of layer	500	750	825	nm	5, Fig. 2
Doping type	Intrinsic				
Doping species	N/A				
Doping/carrier concentration	5x10 ¹⁶		cm ⁻³		
Crystal structure	Wurzite				
Surface crystal orientation	(0,0,0, $\bar{1}$)				
Surface termination	Nitrogen				
Orientation accuracy			±1	degree	
FWHM X-ray ω-scan rocking curve	5		min		
Defect density	<5x10 ⁹		cm ⁻²		
Total Thickness Variation (TTV)			75	nm	2
Top surface RMS roughness	1		1.1	nm	1, Fig. 6
Edge exclusion	0.5		1	mm	4
Allowable temperature for epitaxial growth	1200		°C		

Notes:

1. Root-mean-square roughness is measured using Atomic Force Microscope over a square evaluation surface with sides equal to 1 μm.
2. Over entire wafer less exclusion area.
3. Centerline roughness is the area between the roughness profile and its center line divided by the evaluation surface. Evaluation surface is a 100 μm x 100 μm square.
4. Distance from the edge of wafer from which bow and TTV are measured.
5. Thickness layer is grown to within <5% uniformity, and to within 10% accuracy.

TECHNICAL SPECIFICATIONS (...continued)

	Min	Typical	Max	Units	Notes
Diamond substrate properties					
Crystal structure	Polycrystalline				
Thickness of diamond substrate	20	25	30	μm	
Dielectric Loss tangent @ 140 Ghz	1x10 ⁻⁵				
Optical transparency	Opaque				
Total Thickness Variation (TTV)			5	μm	2
Electrical resistivity	10 ¹³	10 ¹⁶		Ω-cm	
Thermal conductivity	11	12		W/cm/K	
Specific heat		5		J/kg/K	
Thermal expansion coefficient		1.3 ± 0.2 · 10 ⁻⁶		1/K	
Young's Modulus of Elasticity		1,050		GPa	
Vickers Hardness (HV)	60			GPa	
Density		3.5		g/cm ³	
Poisson's Ratio		0.2			
Dielectric Constant @ 1MHz		5.7			
Dielectric Strength		1.0 x 10 ⁷		V/cm	
Tensile Strength		290		kg/mm ²	
Compressive Strength	110			GPa	

Composite Xero wafer properties

Wafer Bow (without Si-handle)	Elastic Flexible	100	μm	6
Wafer Bow (with Si-handle)	15	20	μm	
Wafer's Bow Sense	Concave			Fig. 4
Total Thickness Variation (TTV)		20	nm	2
Proprietary interlayer thickness		0.5	nm	7

Notes:

- The Xero wafer maintains a bow that is flexible. When pressed with a flat surface, the wafer will bounce according to the applied pressure.
- A proprietary interlayer is used to atomically attach GaN to a specially treated CVD diamond substrate. This dielectric interlayer is non-metallic and non-organic.

TECHNICAL SPECIFICATIONS (...continued)

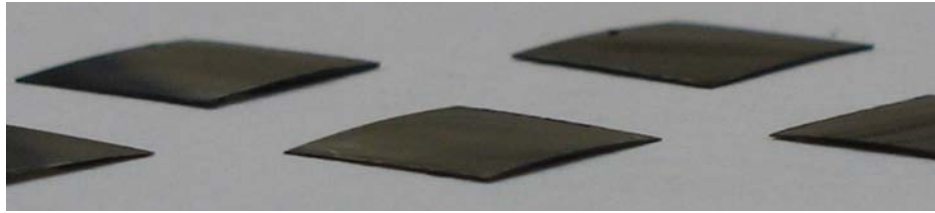


Figure 1 – Optical photograph of Xero wafers at $\sim 30^\circ$ grazing angle

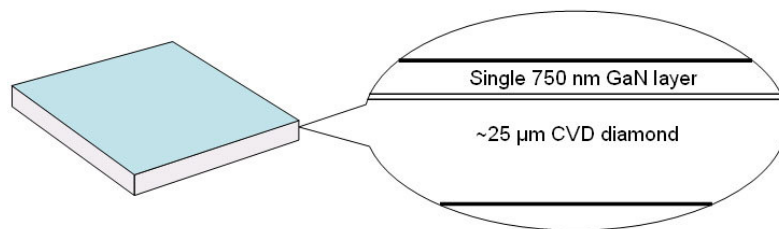


Figure 2 – Schematic of free-standing Xero wafer and cross-section – Option F

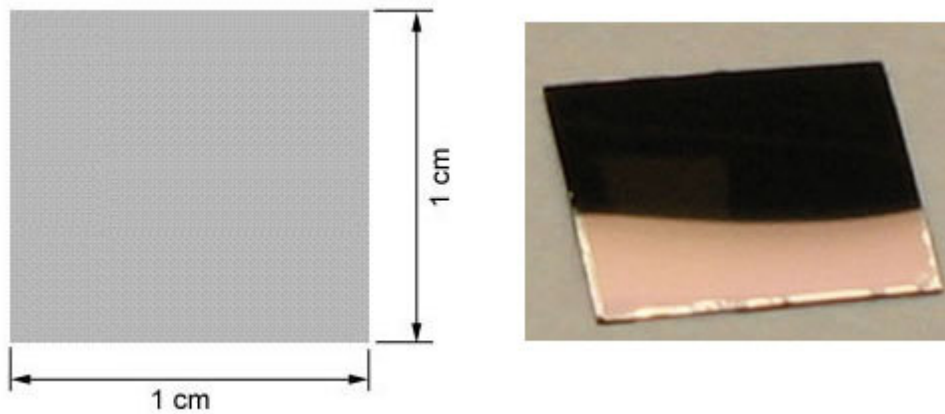


Figure 3 – Wafer dimensions with optical photograph of Xero wafer

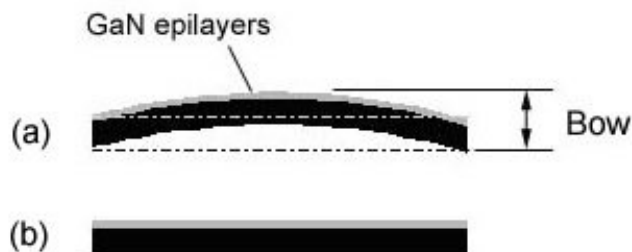


Figure 4 – Xero wafers are bowed as shown with (a), but the bow is elastic and the wafers can be supplied flat as illustrated in (b) and Figure 7; see Ordering Information (pp. 8)

TECHNICAL SPECIFICATIONS (...continued)

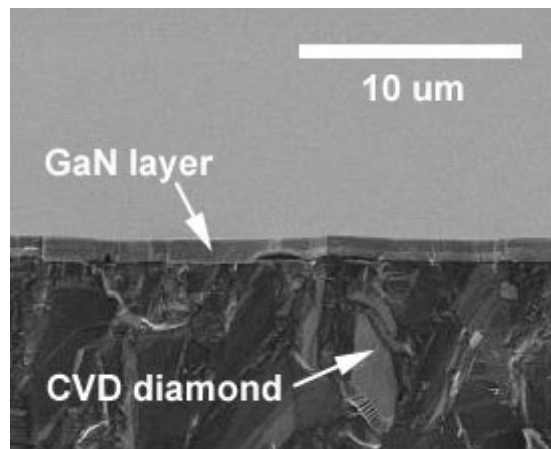


Figure 5 – SEM micrograph of GaN layer on top of CVD diamond

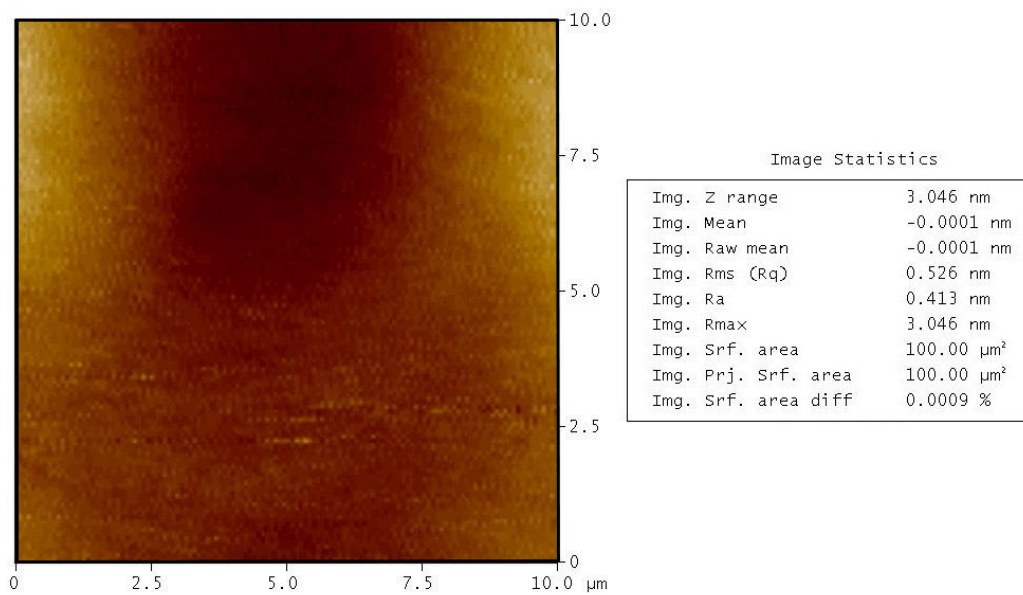


Figure 6 – Atomic Force Microscopy image of the GaN surface

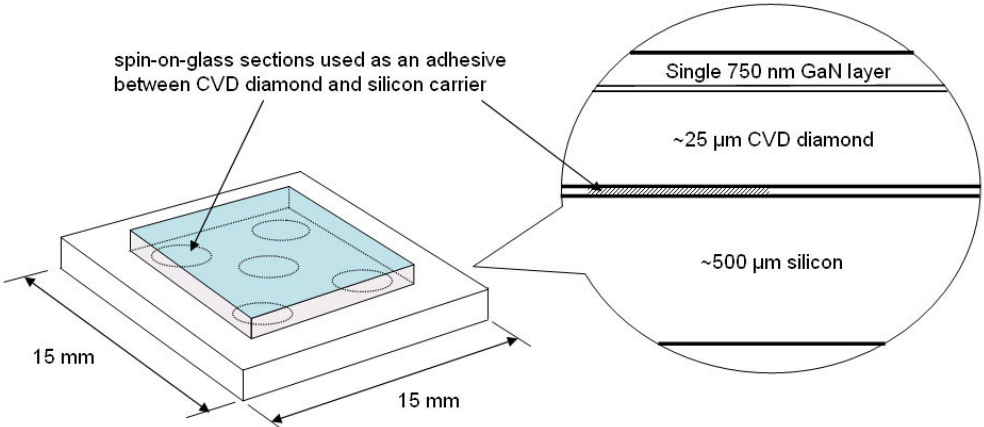
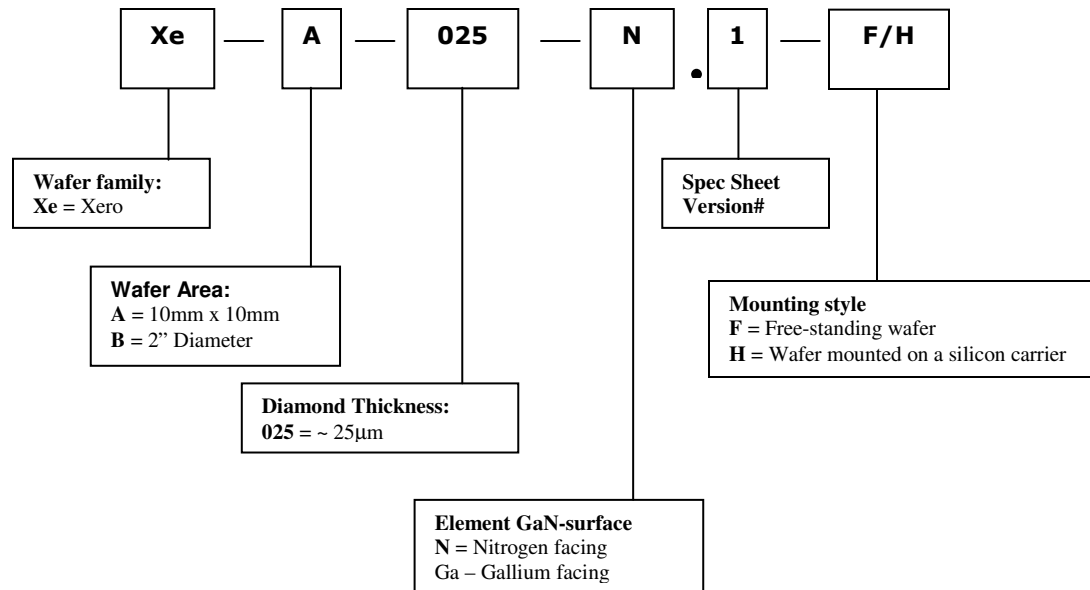


Figure 7 – Schematic of Xero wafer mounted on silicon carrier (handle) – Option H.

General	
Packaging	Wafer tray

ORDERING INFORMATION



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